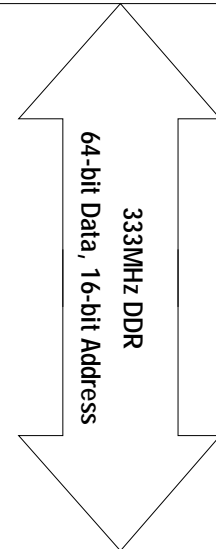


UC Davis ECE MSEE Thesis

DDR2 SDRAM SODIMM INTERPOSER BOARD

Blue = Top-Side (Correct Decal)
 Red = Bottom-Side (Wrong Decal)

Micron
 DDR2 SDRAM
 SODIMM
 Top Side of Board
 MT16HTF25664H – 2GB



Micron
 DDR2 SDRAM
 SODIMM
 Bottom Side of Board
 MT16HTF25664H – 2GB

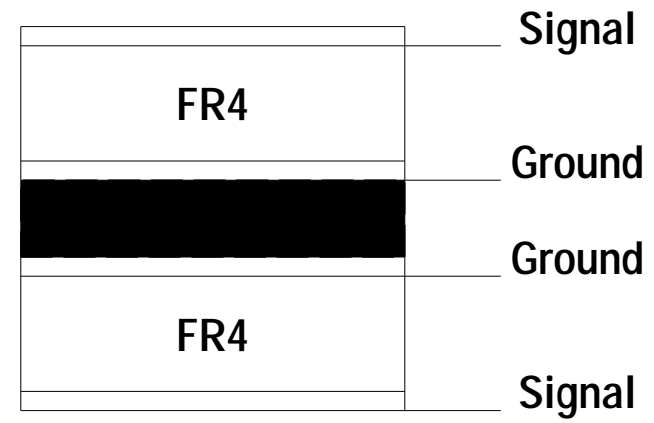


| | | | |
|--------------|----------------|-------------------|----------------|
| Title: | | BLOCK DIAGRAM | |
| File: | | SODIMM_INTERPOSER | |
| Created by: | JEREMY W. WEBB | Date: | 9-21-2009_8:29 |
| Modified by: | | Date: | |
| PCB NO: | 389 | Size: | B |
| Sheet | 1 | of | 4 |
| REV: | 3 | | |

A INDEX

| SHEET/BLOCK | DESCRIPTION |
|-------------|---|
| 1 | TITLE PAGE/BLOCK DIAGRAM |
| 2 | SCHEMATIC DESIGN SHEET INDEX |
| 3 | DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB (TOP - SIDE) |
| 4 | DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB (BOTTOM - SIDE) |

B Board Stack-Up



| | |
|----------------------------|-----------------------------|
| Title: SCHEMATIC INDEX | |
| File: SODIMM_INTERPOSER | |
| Created by: JEREMY W. WEBB | Date: 9-21-2009_8:29 |
| Modified by: | Date: |
| PCB NO: 389 | Size: B Sheet 2 of 4 REV: 3 |

DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB (TOP - SIDE)

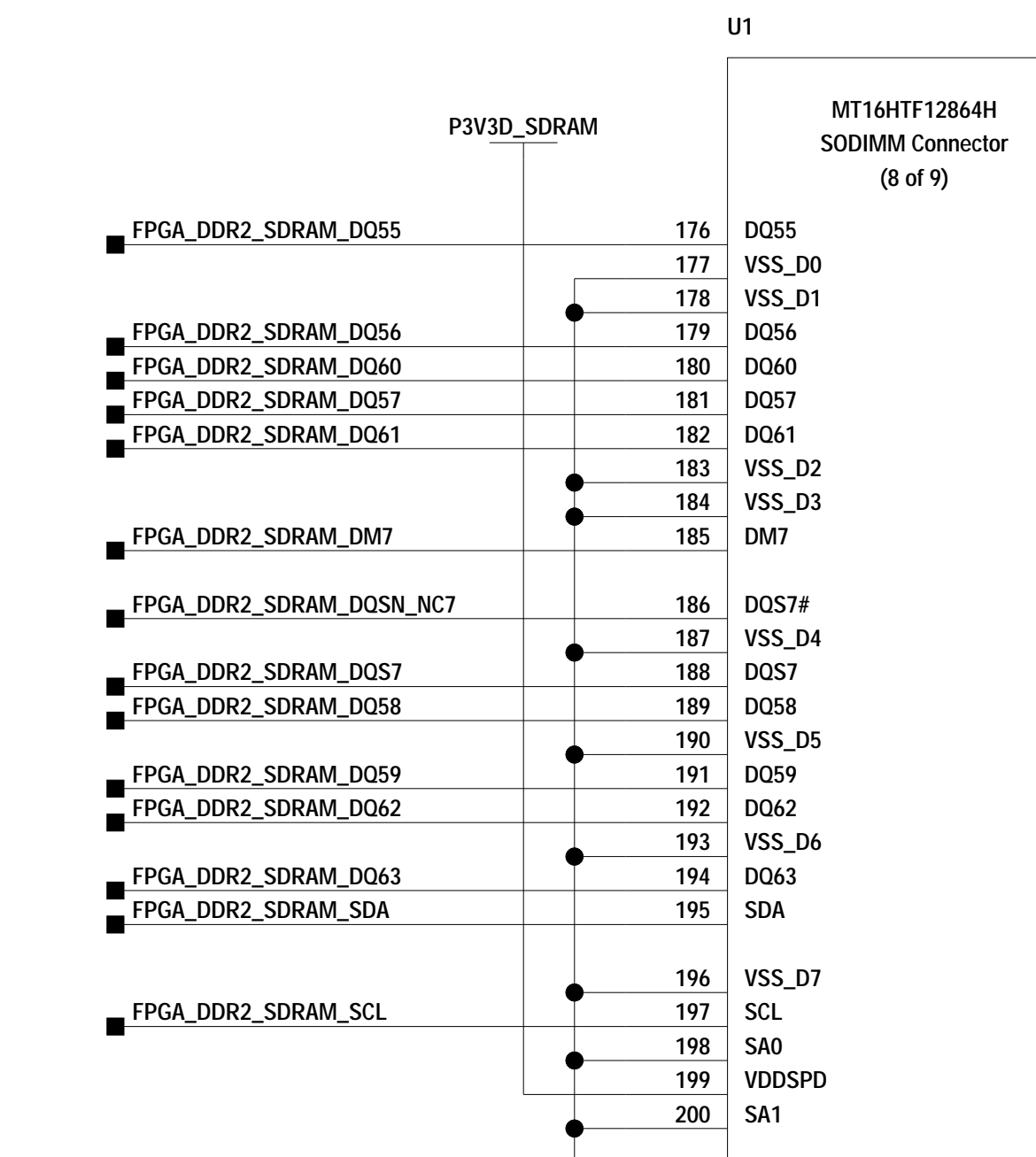
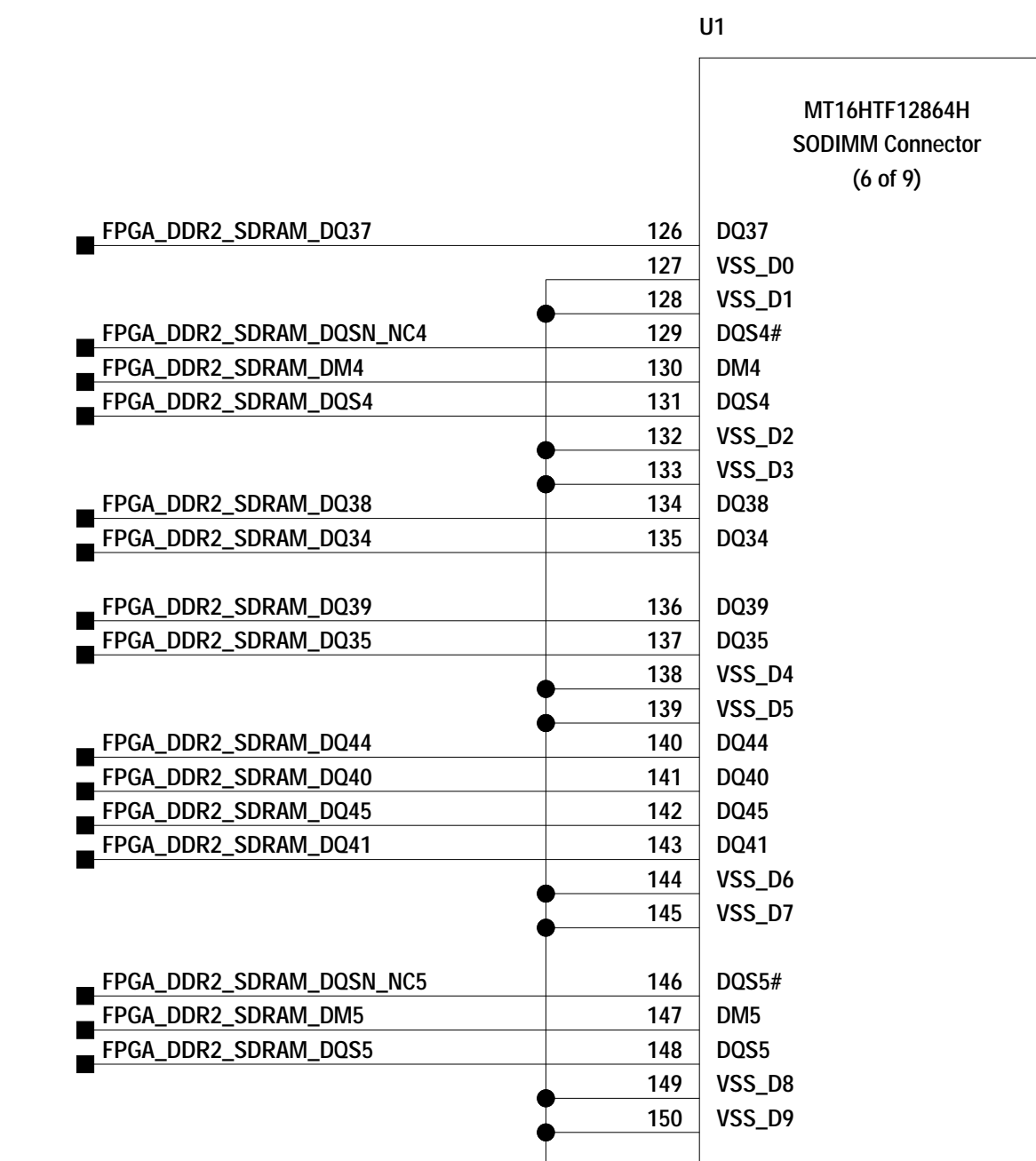
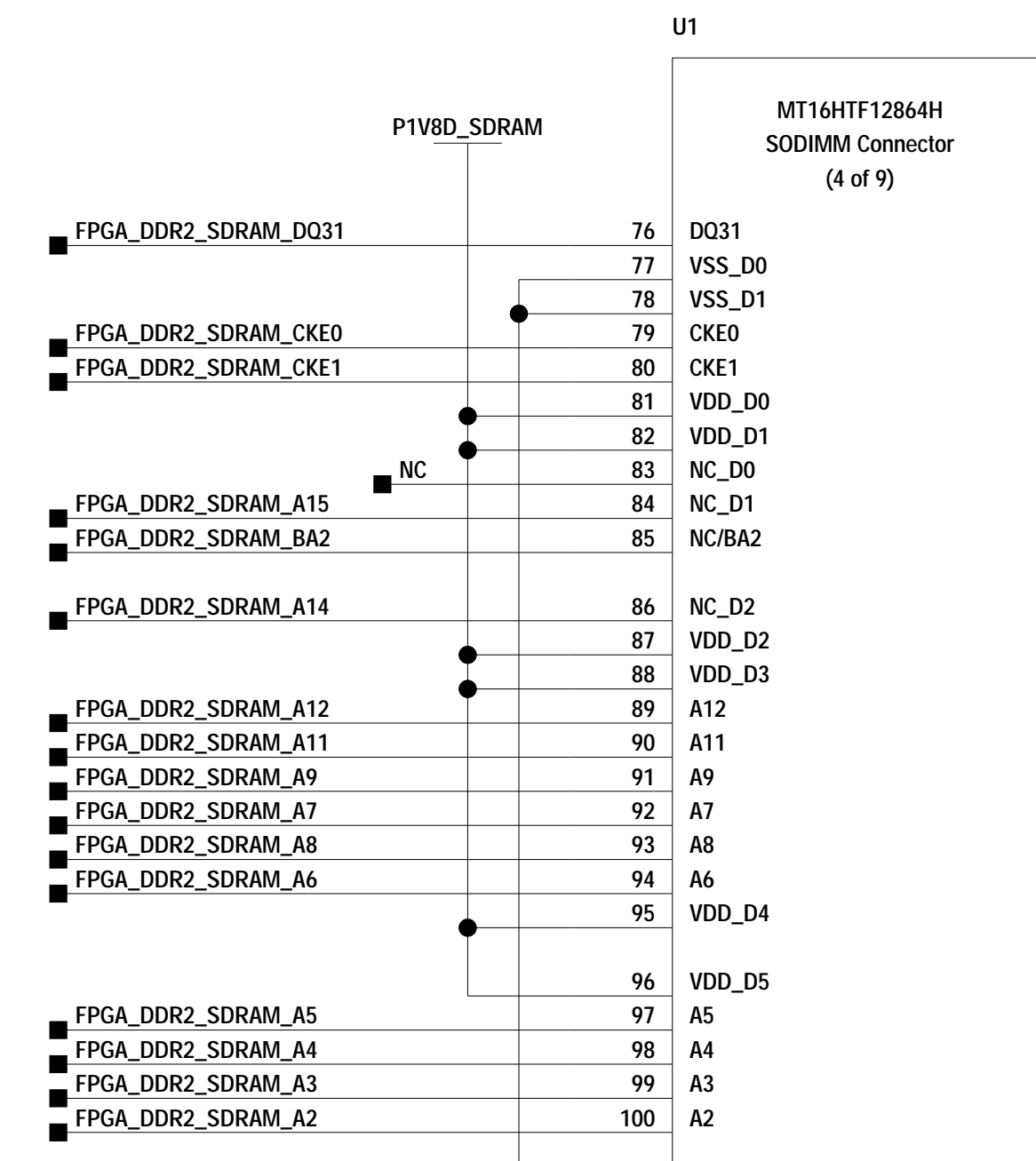
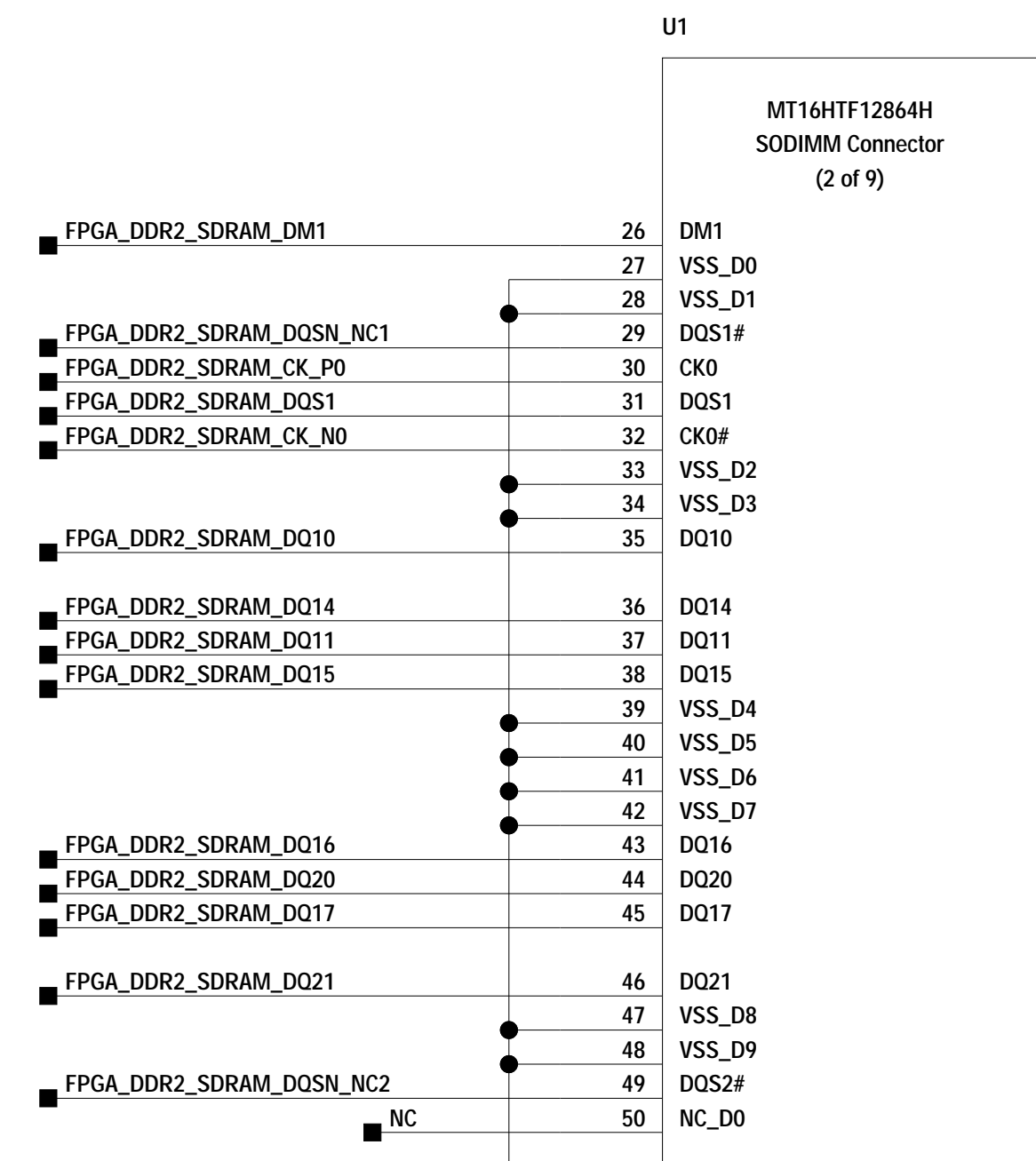
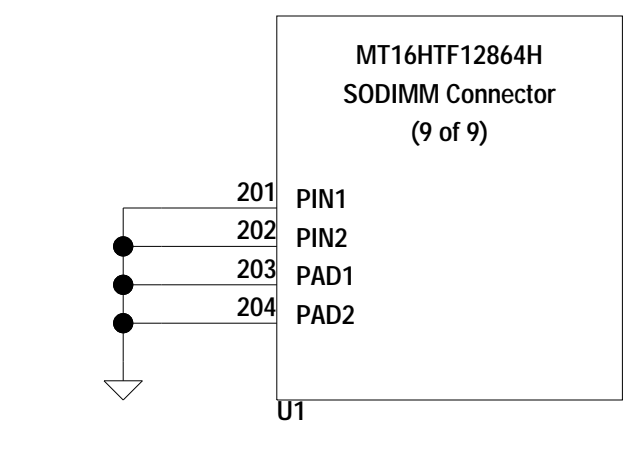
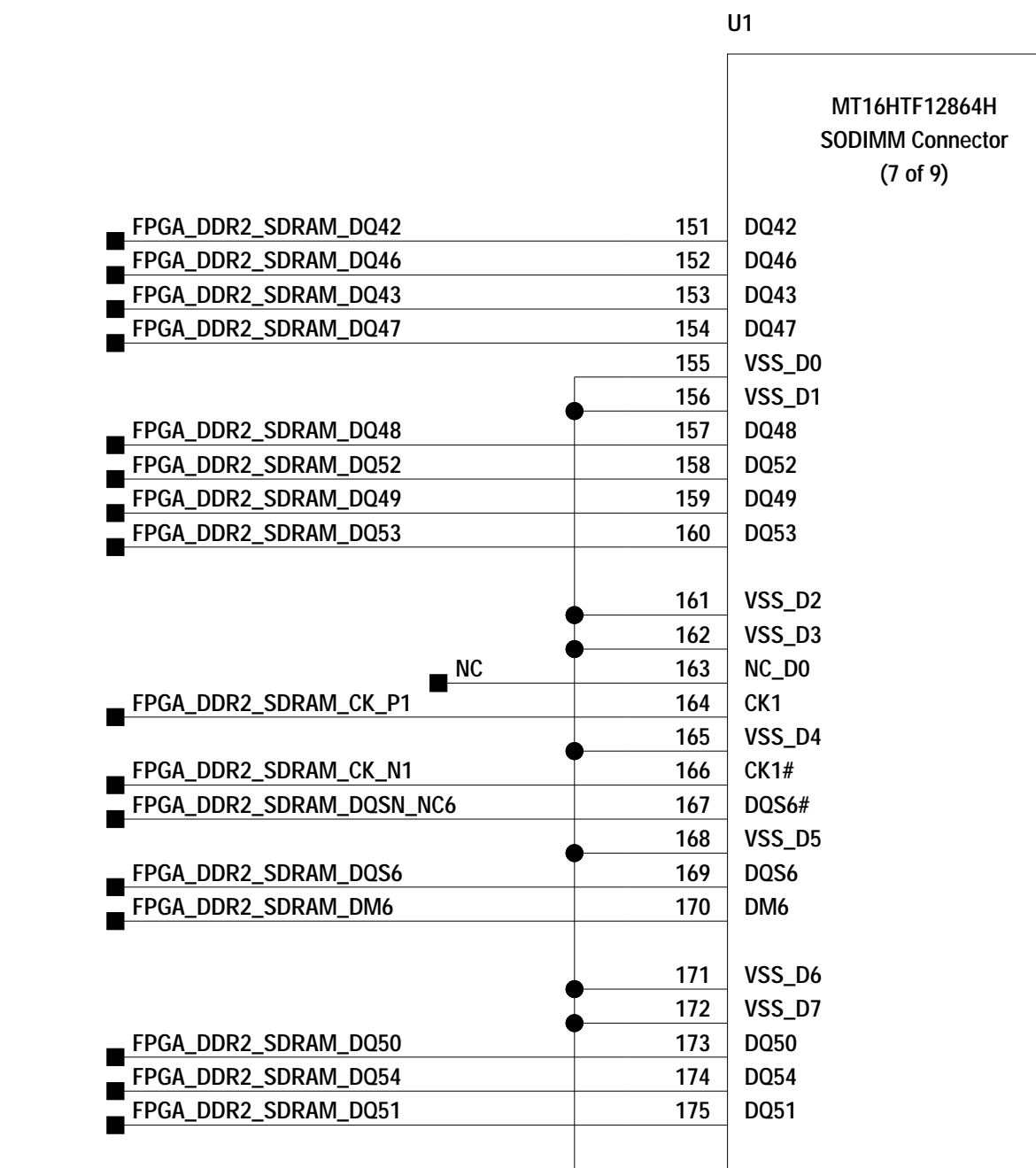
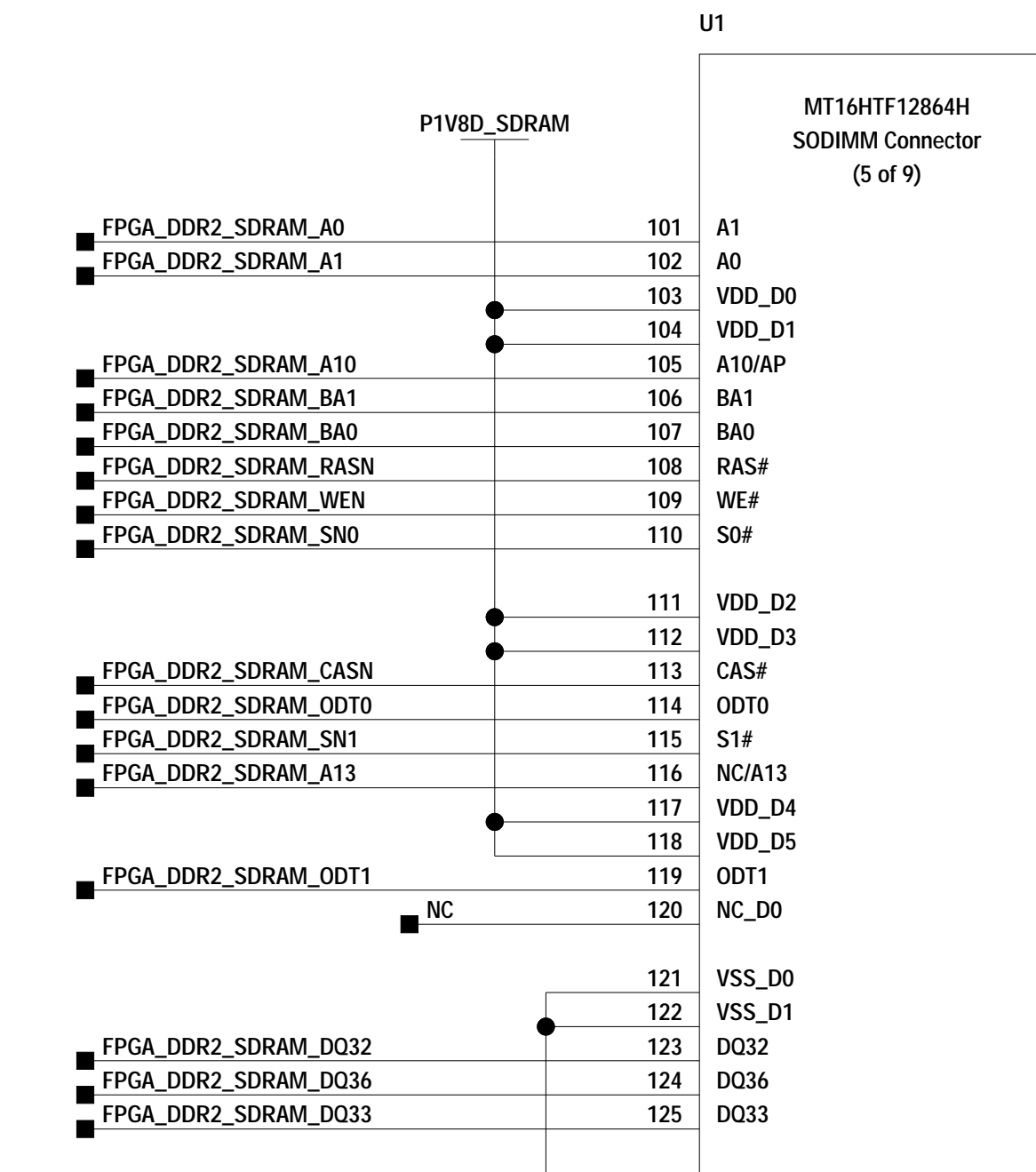
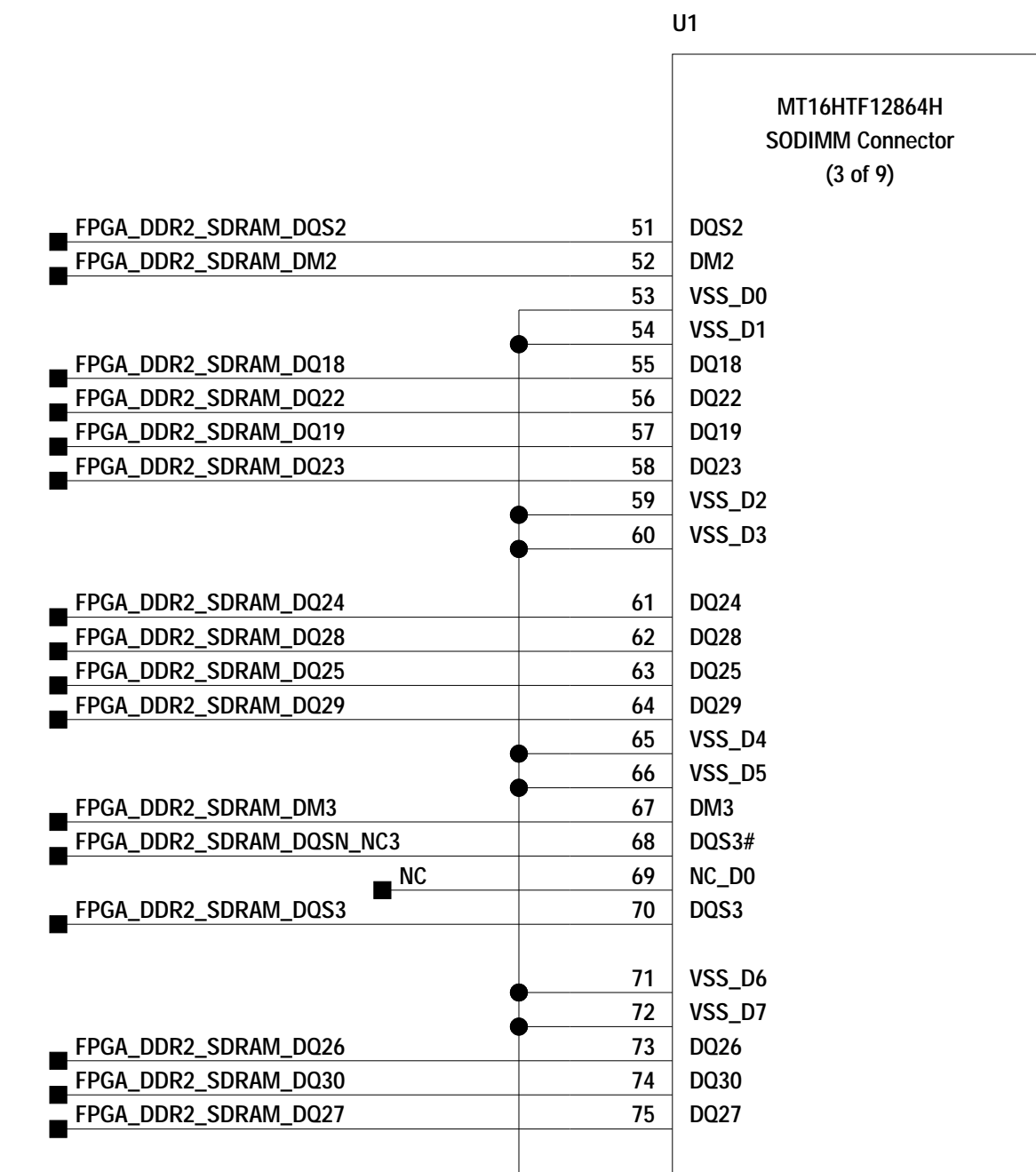
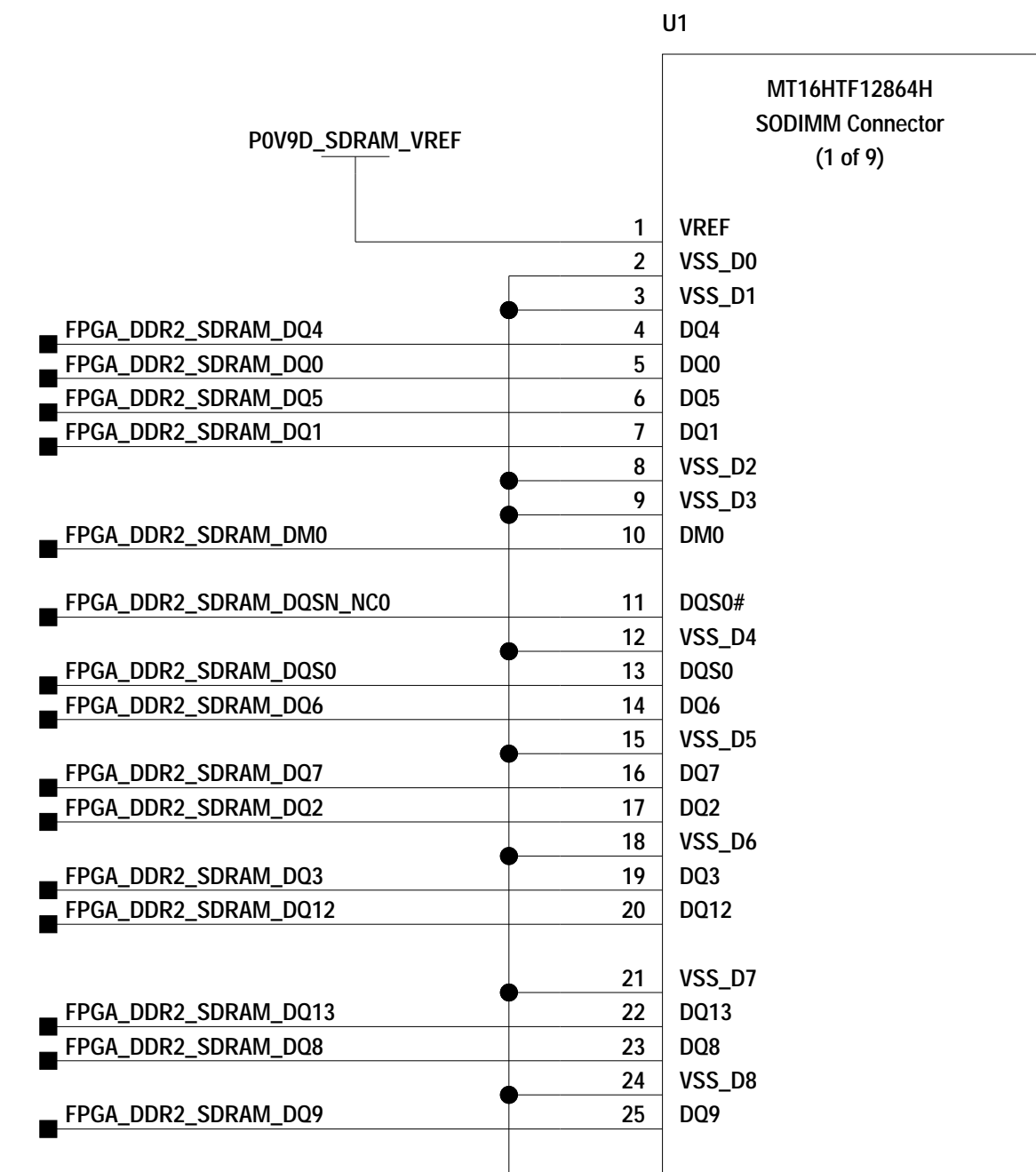
256 Meg x 64-bits

Provides between 1.024 GS and 1.280 GS storage of sampled data.

** INPUTS **

SDRAM Signals

- 3-C1,3-C2,3-C3,3-C4,3-D1 ○ FPGA_DDR2_SDRAM_D06[3:0]
- 3-D2,3-D3,3-D4,3-E1
- 3-F4,4-C1,4-C2,4-C3
- 4-C4,4-D1,4-D2,4-D3
- 4-D4,4-E1,4-E4
- 3-C2,3-D3,3-E1,3-E3,4-C2
- 4-D3,4-E1,4-E3
- FPGA_DDR2_SDRAM_A15[0]
- 3-C2,3-D3,3-E1,4-C2,4-D3
- 4-E1
- FPGA_DDR2_SDRAM_BA[2:0]
- 3-D3,3-E1,4-D3,4-E1
- FPGA_DDR2_SDRAM_RASN
- 3-D3,3-E1,4-D3,4-E1
- FPGA_DDR2_SDRAM_CASN
- 3-D3,3-E1,4-D3,4-E1
- FPGA_DDR2_SDRAM_WEN
- 3-C2,3-E1,4-C2,4-E1
- FPGA_DDR2_SDRAM_CKE[1:0]
- 3-C1,3-C3,3-C4,3-D1,3-D2
- 3-D4,3-E1,3-E2,4-C1
- 4-C3,4-C4,4-D1,4-D2
- 3-C1,3-C3,3-D1,3-D2,3-E2
- 3-D4,3-E1,4-C1,4-C3
- 4-C4,4-D1,4-D2,4-D4
- 4-E1
- FPGA_DDR2_SDRAM_CK_P[1:0]
- 3-C1,3-D4,3-E1,4-C1,4-D4
- 4-E1
- FPGA_DDR2_SDRAM_CK_N[1:0]
- 3-C1,3-D4,3-E1,4-C1,4-D4
- 4-E1
- FPGA_DDR2_SDRAM_DM[7:0]
- 3-C1,3-C3,3-C4,3-D1,3-D2
- 3-D4,3-E1,3-E2,4-C1
- 4-C3,4-C4,4-D1,4-D2
- 4-D4,4-E1,4-E2
- FPGA_DDR2_SDRAM_SNI[1:0]
- 3-D1,3-D3,4-D1,4-D3
- FPGA_DDR2_SDRAM_ODT[1:0]
- 3-C4,3-D1,4-C4,4-D1
- FPGA_DDR2_SDRAM_SDA
- 3-C4,3-D1,4-C4,4-D1
- FPGA_DDR2_SDRAM_SCL



VLSI Computation LAB

Title: DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB (TOP - SIDE)
 File: SODIMM_INTERPOSER
 Created by: JEREMY W. WEBB Date: 9-21-2009_8:29
 Modified by: Date:
 PCB NO: 389 Size: E Sheet 3 of 4 REV: 3

DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB (BOTTOM - SIDE)

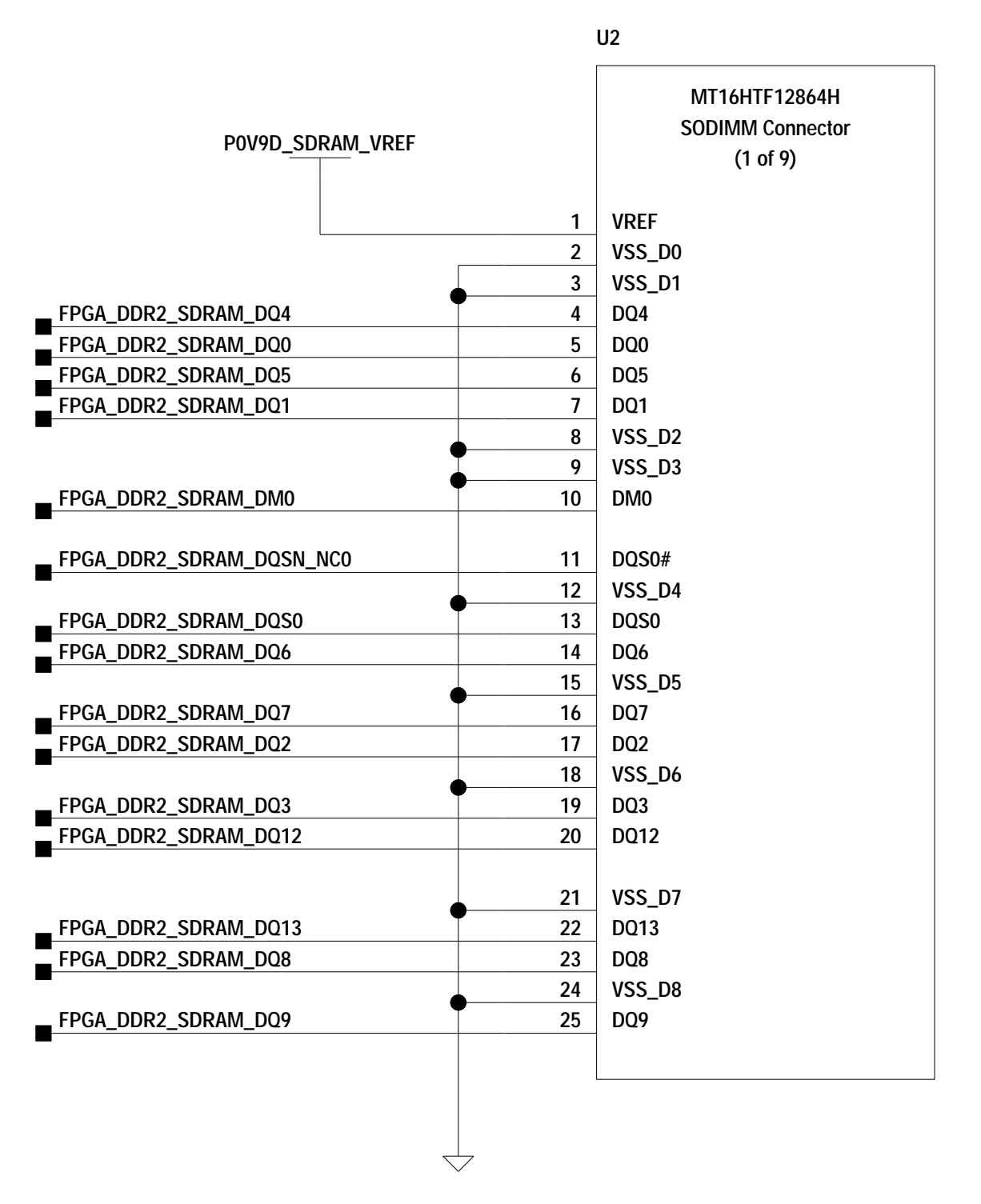
256 Meg x 64-bits

Provides between 1.024 GS and 1.280 GS storage of sampled data.

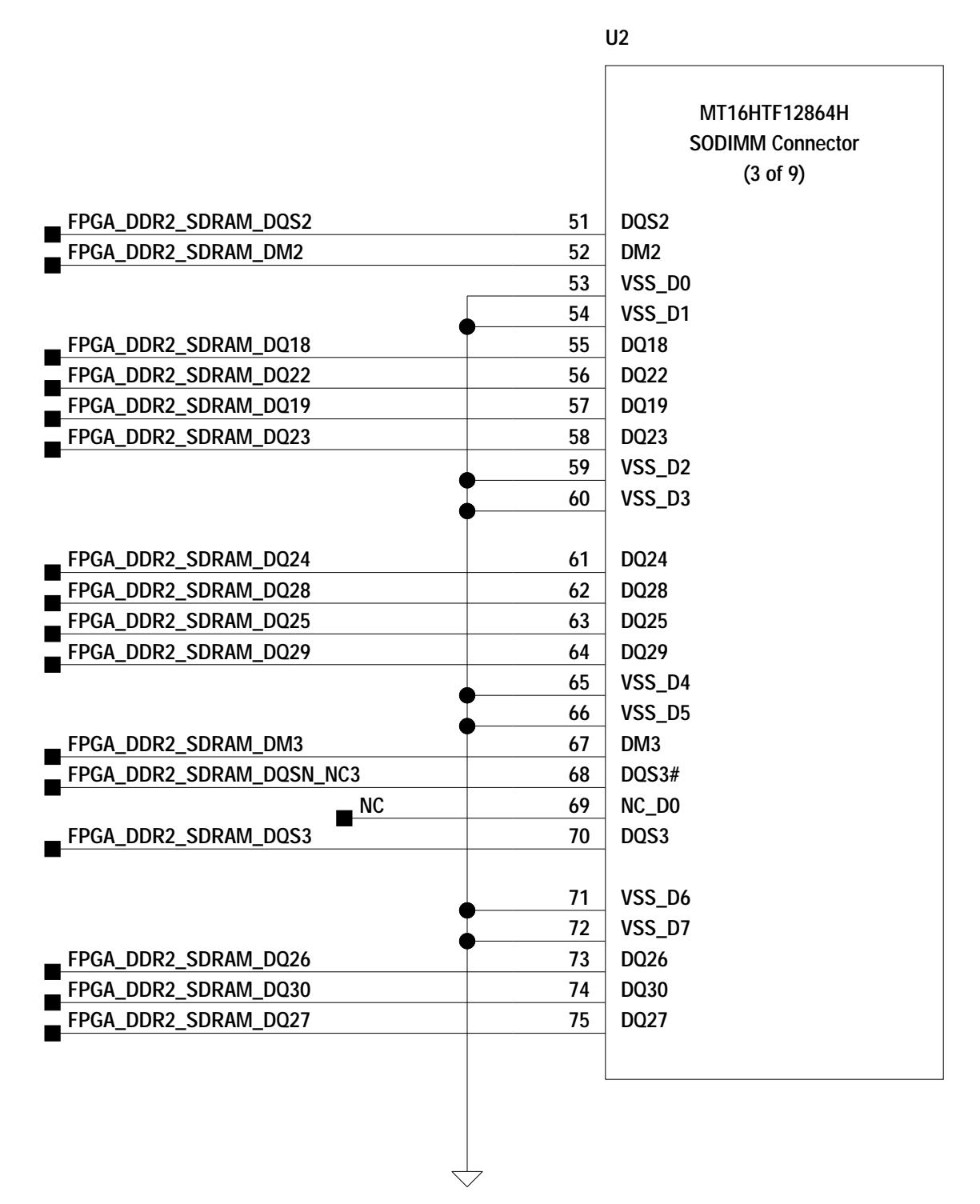
**** INPUTS ****

SDRAM Signals

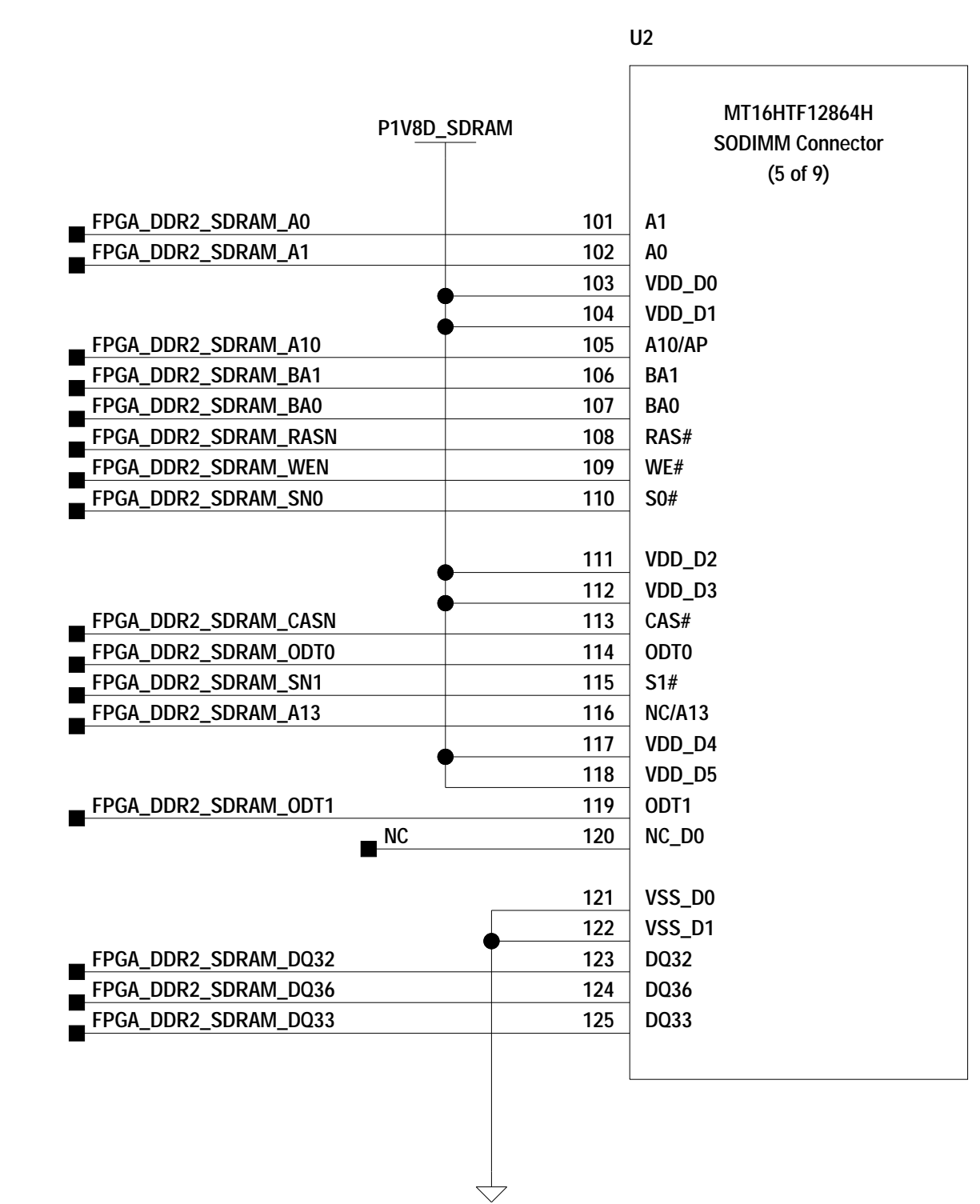
| | |
|--------------------------|---------------------------|
| 3-C1,3-C2,3-C3,3-C4,3-D1 | FPGA_DDR2_SDRAM_D06[3:0] |
| 3-D2,3-D3,3-D4,3-E1 | FPGA_DDR2_SDRAM_D06[3:0] |
| 3-E4,4-C1,4-C2,4-C3 | FPGA_DDR2_SDRAM_D06[3:0] |
| 4-C4,4-D1,4-D2,4-D3 | FPGA_DDR2_SDRAM_D06[3:0] |
| 4-D4,4-E1,4-E4 | FPGA_DDR2_SDRAM_D06[3:0] |
| 3-C2,3-D3,3-E1,3-E3,4-C2 | FPGA_DDR2_SDRAM_A15[0] |
| 4-D3,4-E1,4-E3 | FPGA_DDR2_SDRAM_A15[0] |
| 3-C2,3-D3,3-E1,4-C2,4-D3 | FPGA_DDR2_SDRAM_BA[2:0] |
| 4-E1 | FPGA_DDR2_SDRAM_BA[2:0] |
| 3-D3,3-E1,4-D3,4-E1 | FPGA_DDR2_SDRAM_CASN |
| 3-D3,3-E1,4-D3,4-E1 | FPGA_DDR2_SDRAM_CASN |
| 3-D3,3-E1,4-D3,4-E1 | FPGA_DDR2_SDRAM_WEN |
| 3-C2,3-E1,4-C2,4-E1 | FPGA_DDR2_SDRAM_CKE1[1:0] |
| 3-C1,3-C3,3-C4,3-D1,3-D2 | FPGA_DDR2_SDRAM_DQS[7:0] |
| 3-D4,3-E1,3-E2,4-C1 | FPGA_DDR2_SDRAM_DQS[7:0] |
| 3-C1,3-C3,3-D1,3-D2,3-E1 | FPGA_DDR2_SDRAM_DQS[7:0] |
| 3-D4,3-E1,3-E2,4-C1 | FPGA_DDR2_SDRAM_DQS[7:0] |
| 3-C1,3-C3,3-C4,3-D1,3-D2 | FPGA_DDR2_SDRAM_DM[7:0] |
| 3-D4,3-E1,3-E2,4-C1 | FPGA_DDR2_SDRAM_DM[7:0] |
| 3-C1,3-C3,3-C4,3-D1,3-D2 | FPGA_DDR2_SDRAM_DM[7:0] |
| 3-D4,3-E1,3-E2,4-C1 | FPGA_DDR2_SDRAM_DM[7:0] |
| 3-D1,3-D3,4-D1,4-D3 | FPGA_DDR2_SDRAM_SNI[1:0] |
| 3-D1,3-D3,4-D1,4-D3 | FPGA_DDR2_SDRAM_SNI[1:0] |
| 3-C4,3-D1,4-C4,4-D1 | FPGA_DDR2_SDRAM_SDA |
| 3-C4,3-D1,4-C4,4-D1 | FPGA_DDR2_SDRAM_SCL |



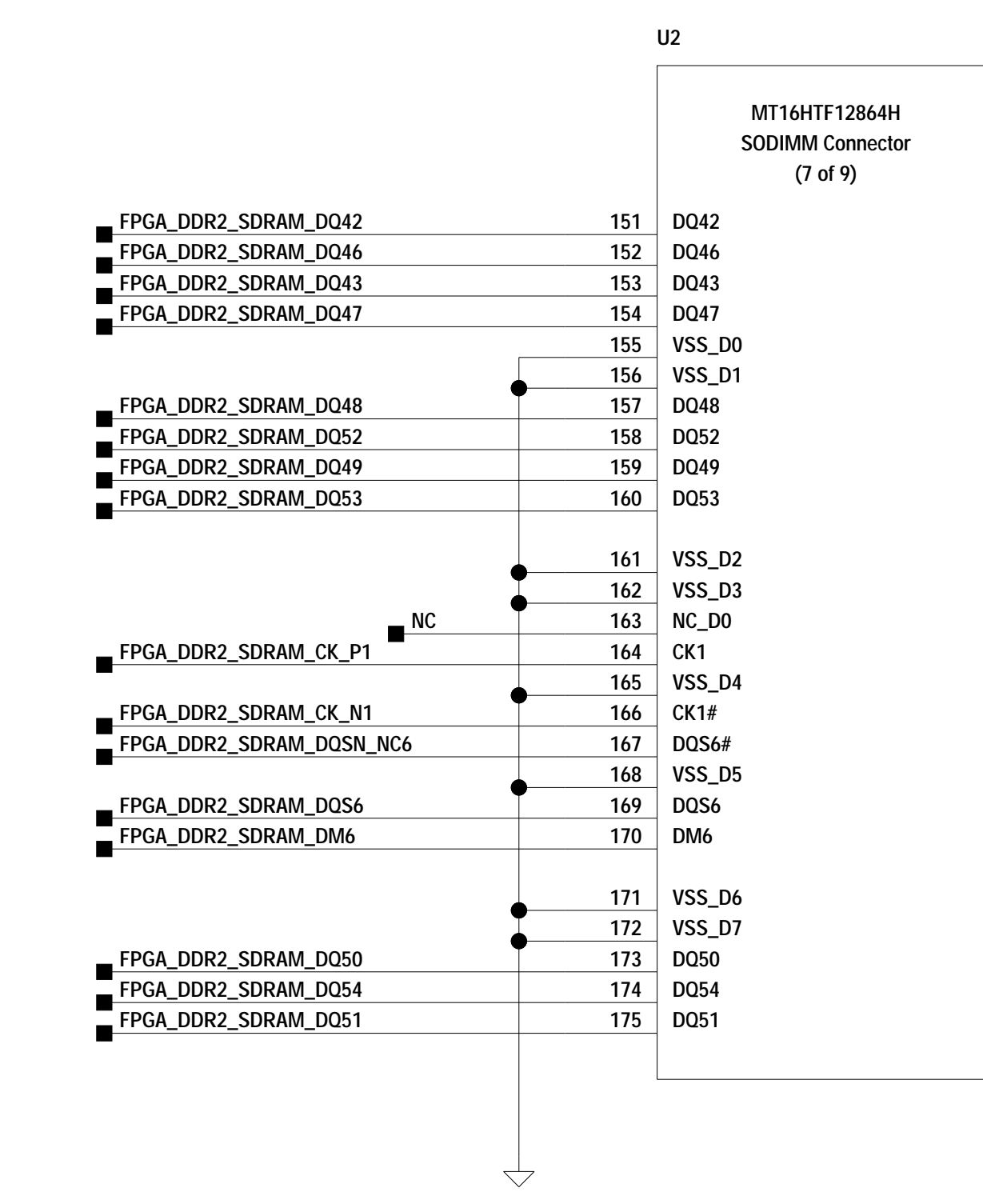
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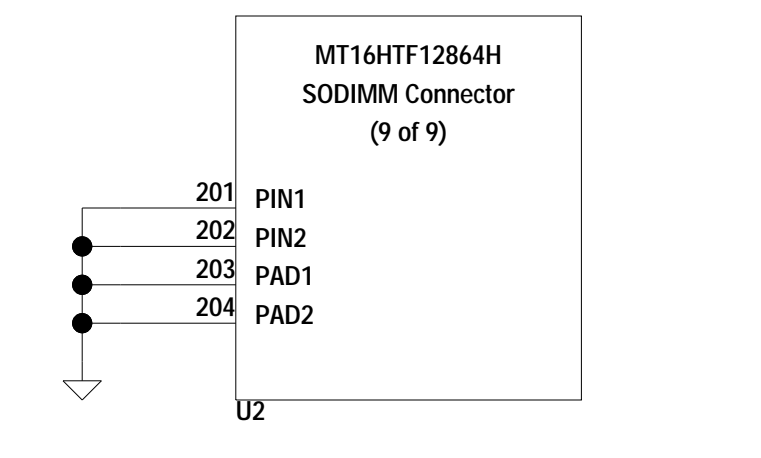
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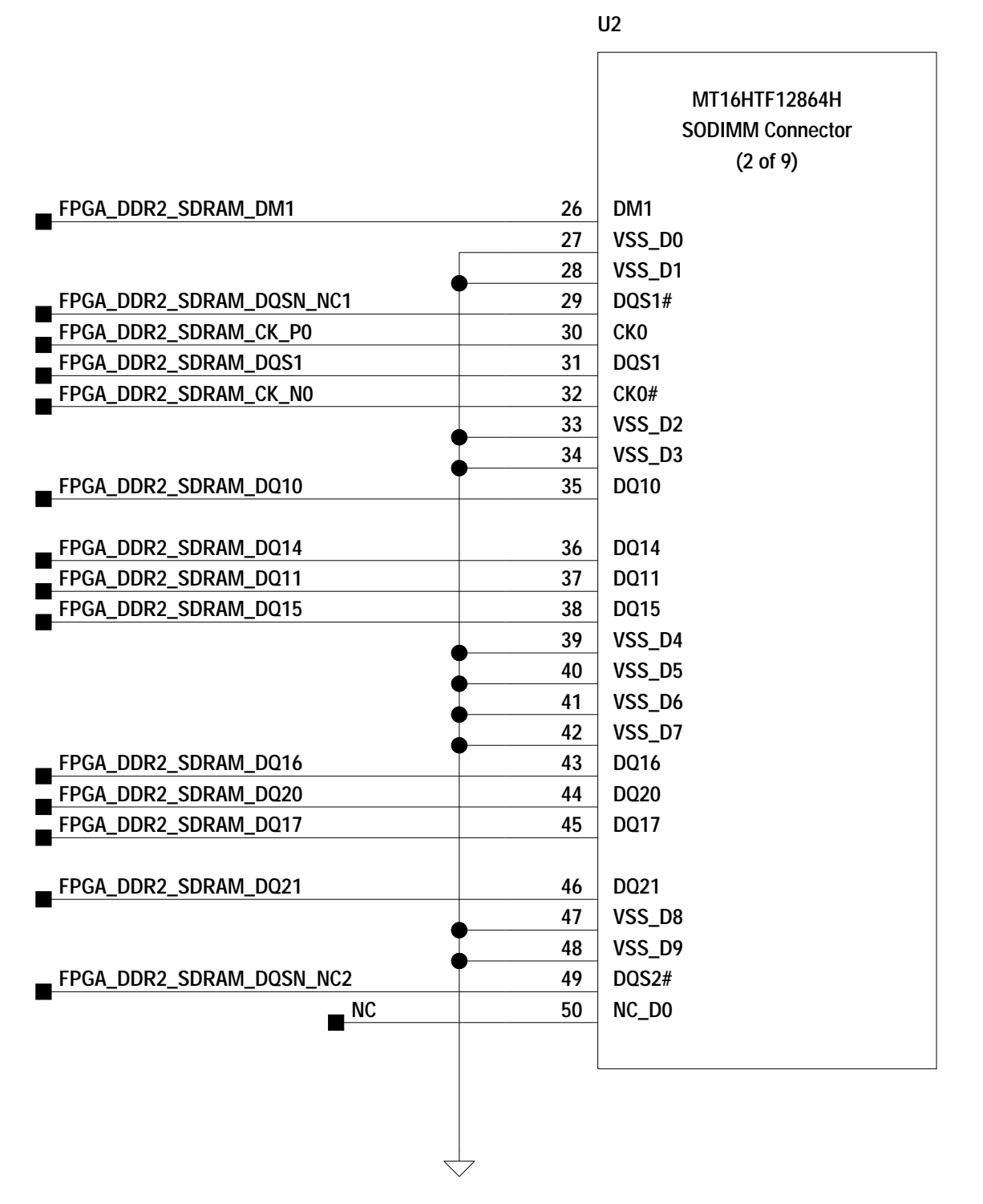
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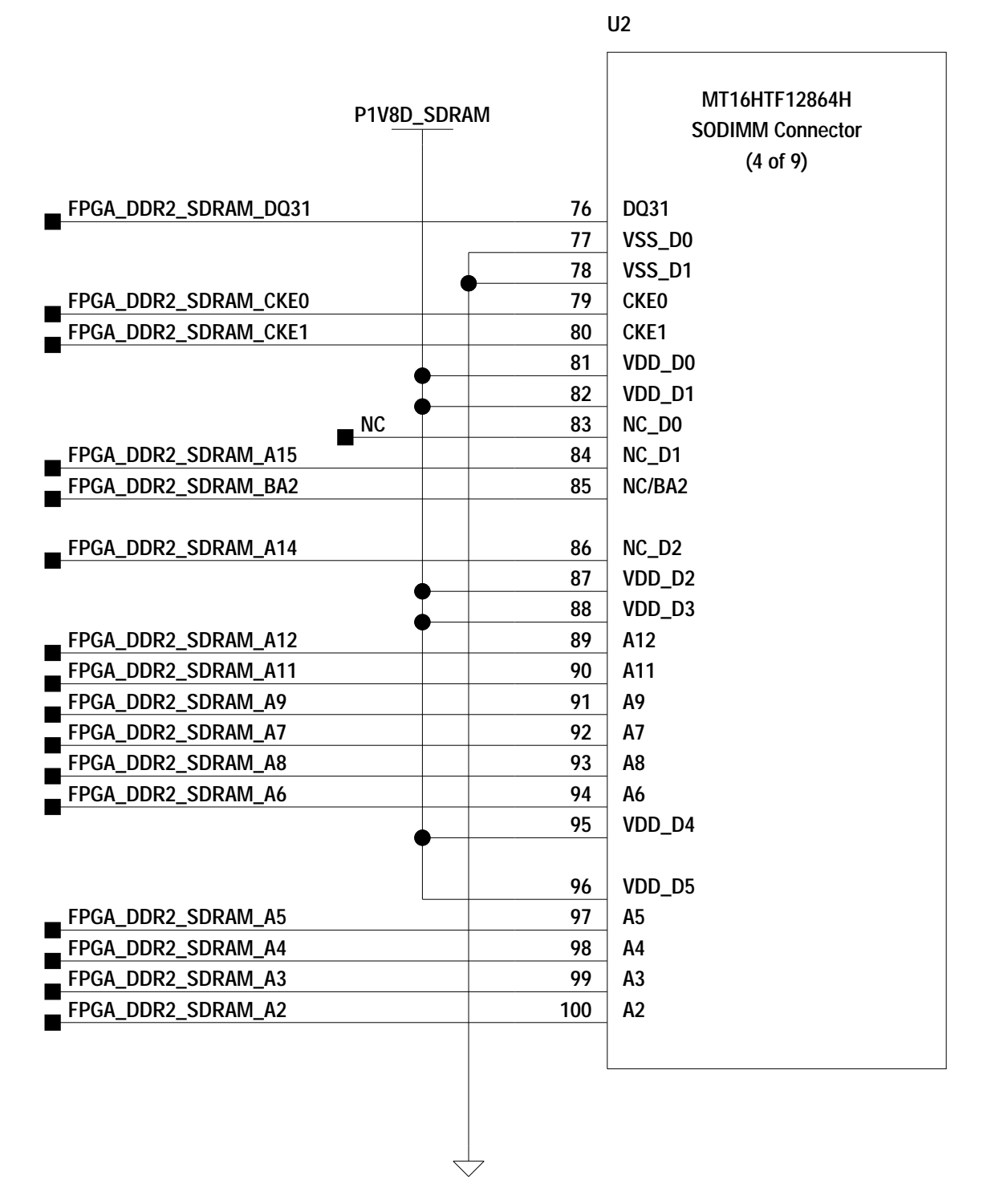
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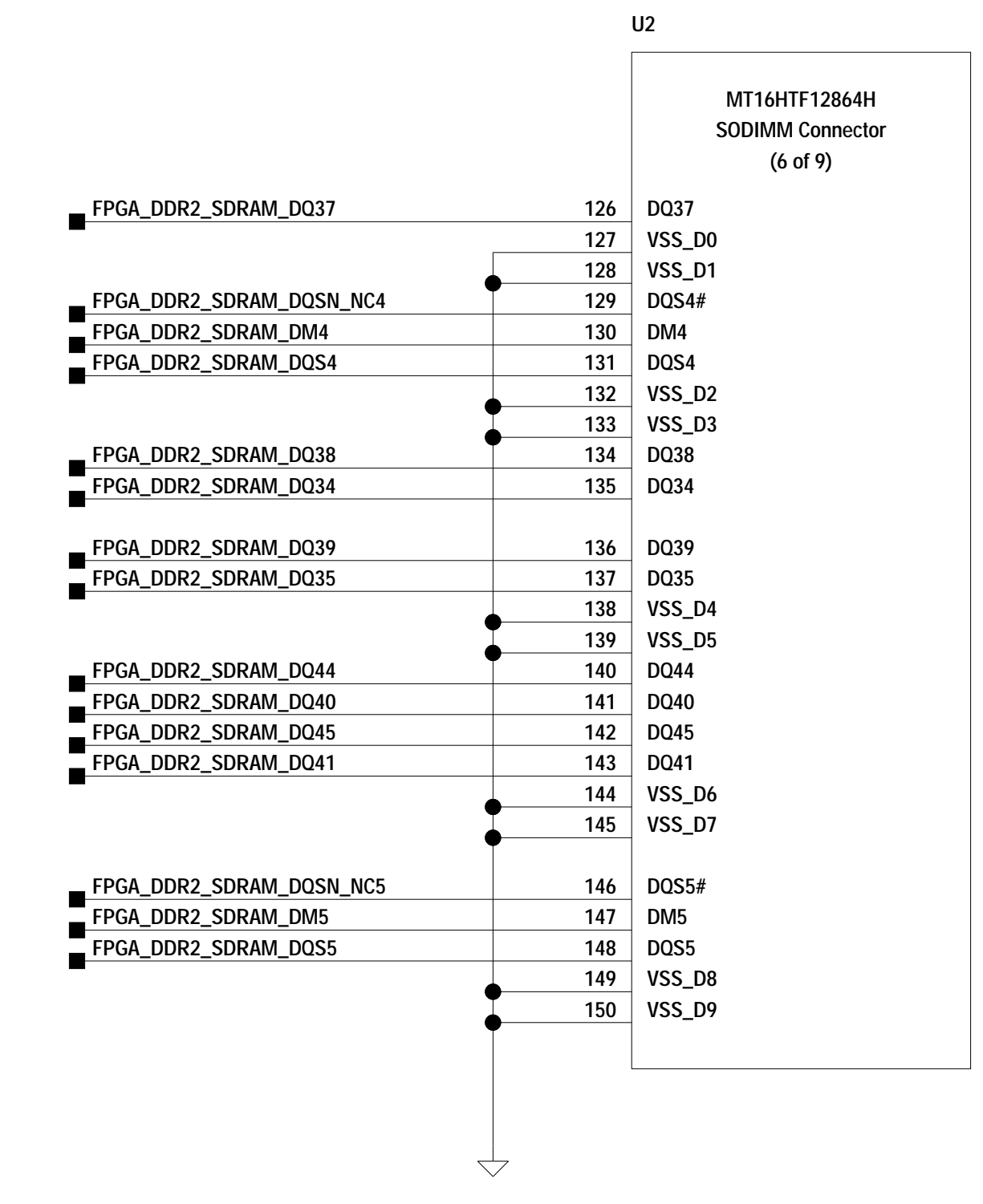
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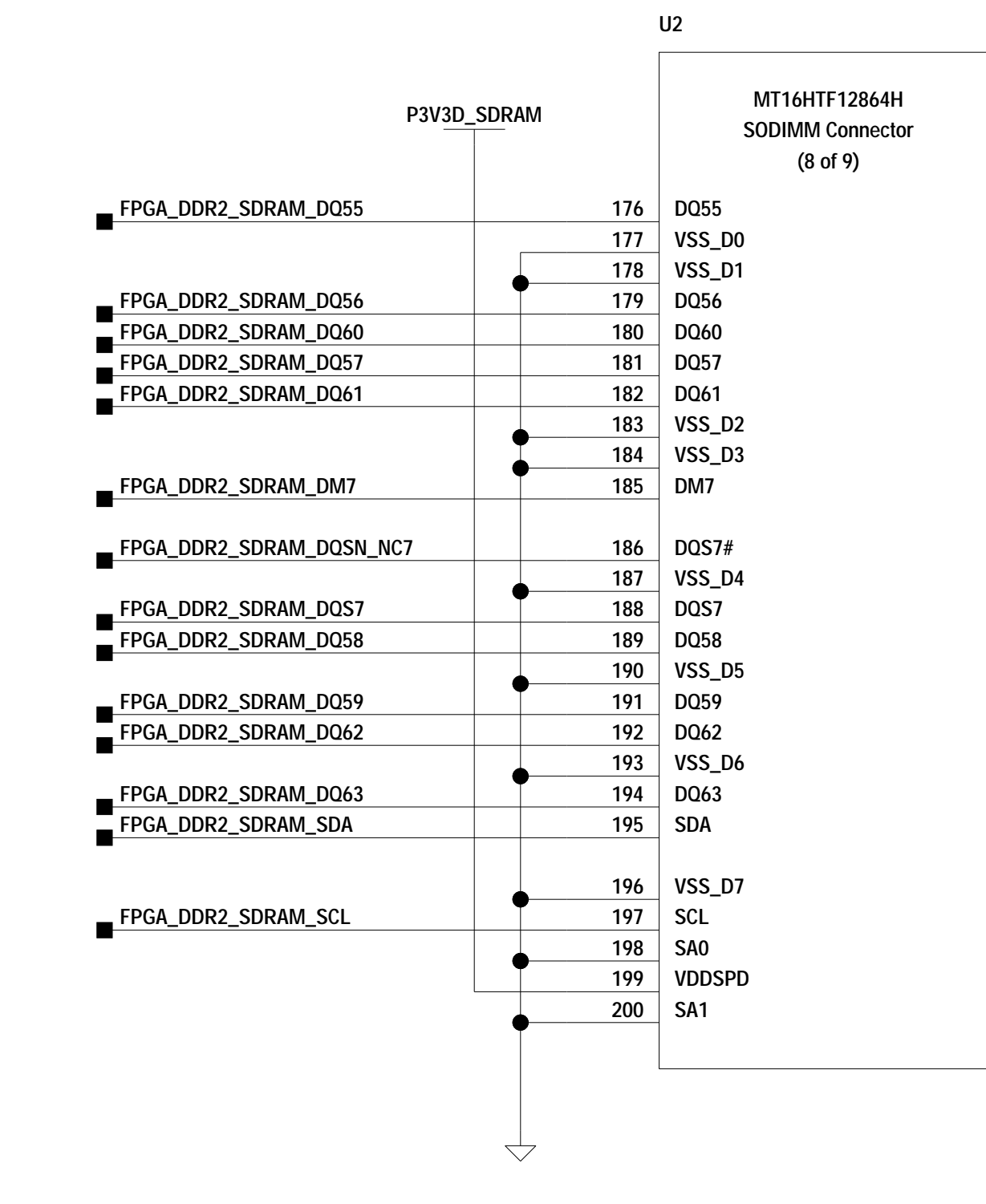
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FOOTPRINT=MM50-200_MISSING_OFFSET_MIRRORED



FOOTPRINT=MM50-200_MISSING_OFFSET_MIRRORED



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