

Overview

This document describes a WebServer reference design using the Xilinx MicroBlaze™ soft processor core running at 50 MHz on the Memec Spartan-3 MB (3SMB) development board. The 3SMB development board is designed with DDR SDRAM and an Ethernet PHY.

Experiment Setup

Software

The recommended software setup for this reference design is:

- Windows2000 or WindowsXP
- Xilinx ISE 8.1i (Foundation or BaseX) with latest Service Pack¹
- Xilinx EDK 8.1 with latest Service Pack¹

Hardware

The hardware setup used by this reference design includes:

- Computer with a recommended minimum of 1GB RAM and 1 GB Virtual Memory²
- Memec Spartan-3 MB Development Kit
- Platform USB Cable or JTAG Programming Cable IV
- Serial Cable
- Ethernet cable

MicroBlaze Platform

The design and optimization of the MicroBlaze platform used in this reference design is described in *Building and Optimizing a MicroBlaze BSB System for Spartan-3 MB*. Please refer to that document for a detailed description of how to create the platform. There is no difference between the hardware platform in this design and the result of that tutorial.

In addition to the two applications automatically generated by Base System Builder (BSB), the software platform has had four software applications added to it:

- Running from DDR with no linker
- Running from DDR with a linker
- Testing the Flash
- WebServer

¹ Latest Service Packs are available at www.support.xilinx.com/swupdate

² Refer to the *ISE 8.1i Release Notes and Installation Guide* <http://toolbox.xilinx.com/docsan/xilinx8/books/docs/im/im.pdf>

The WebServer application is described in this document. The other applications are described in the two other documents related to this hardware platform. Additionally, the *Using Memory* document also describes how to create a bootloader.

Additionally, the XilNet and XilMFS libraries have been added to the software platform for the WebServer.

Understanding the Hardware Platform

A block diagram of the hardware platform is shown in Figure 1. Besides the MicroBlaze processor and busses, the design consists of 16 KB local memory, 32 MB DDR, 4 MB Flash, Ethernet MAC, timer, interrupt controller, two UARTs, a debug peripheral (MDM) and multiple GPIOs.

An asynchronous DDR memory controller is used in this design. This allows the MicroBlaze system to run at a lower speed of 50 MHz, which is more reasonable for Spartan-3, while the DDR is running at 75 MHz, which is the minimum required frequency for the Micron DDR. The on-chip Digital Clock Manager (DCM) is used to create the various clock frequencies and phases required to make this system work, all based on the 75 MHz oscillator on the 3SMB board.

Since the OPB_ETHERNET core runs at the same speed as the OPB and MicroBlaze, which is 50 MHz. At this frequency, only 10Mbps operation is supported. The webserver code provides the necessary setup to the BCM5221 PHY to force 10 Mbps operation. Without this, the PHY is capable of negotiating a 100 Mbps link, but the OPB_ETHERNET would not function.

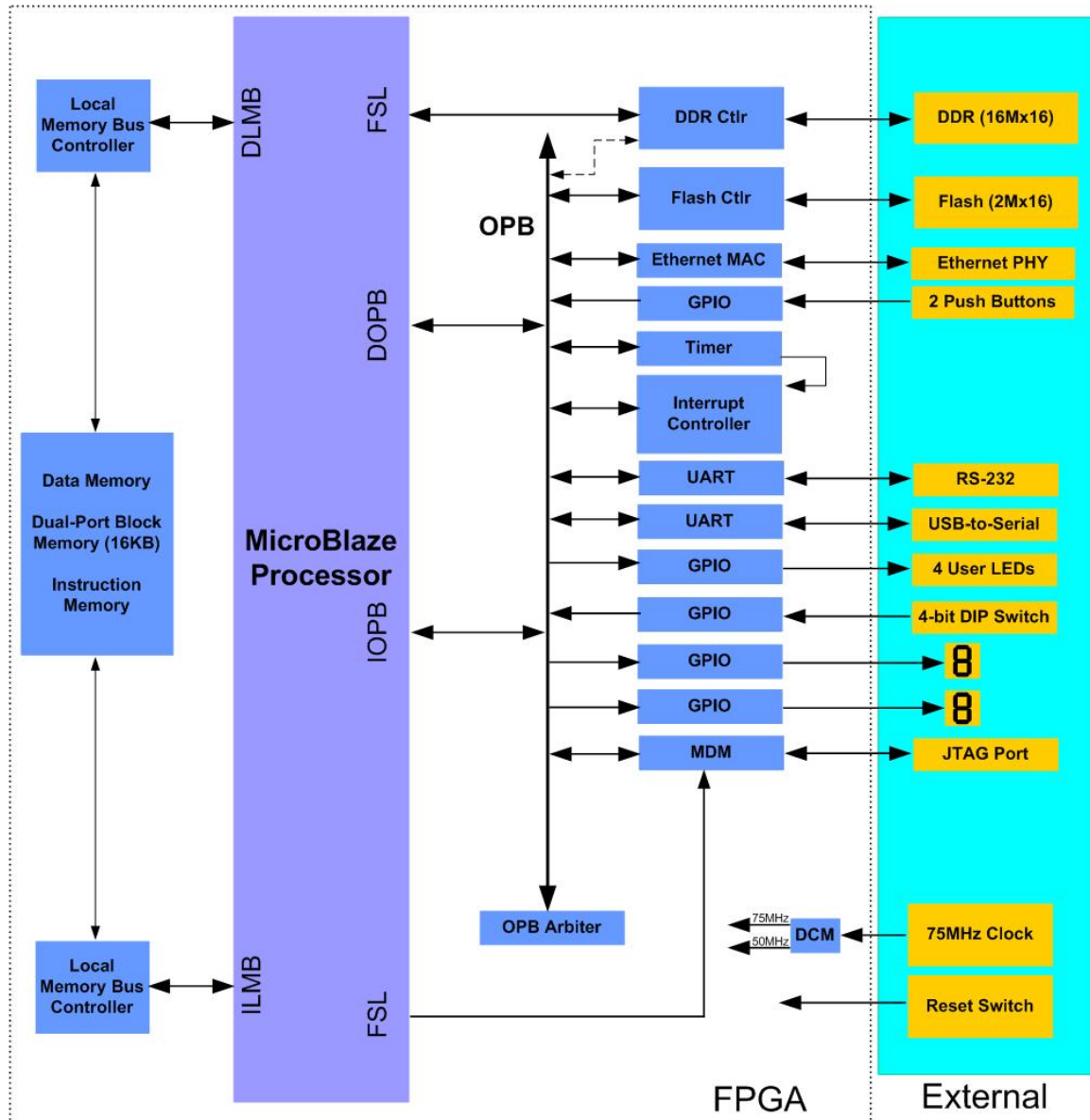
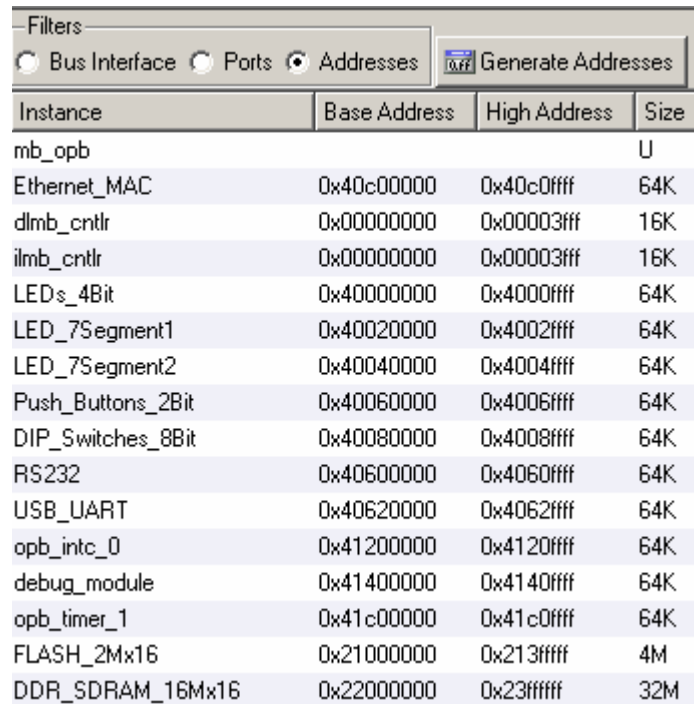


Figure 1 – Block Diagram of BSB-Generated System

Note on licensing: The 10/100 Ethernet MAC OPB peripheral is not a free core. An evaluation license is required to use the core. The evaluation version of the core includes built-in timeout circuitry that will disable the core after a period of time. The evaluation version of the core is included in EDK. This example will work for some time with the default EDK installation. However, those intending to use the core in production should contact their local Memec distributor to purchase a full license for the core.

Memory Map

The memory map is auto-generated by BSB. This memory map can be edited manually, re-generated, or simply viewed by selecting the *Addresses* radio button in the System Assembly view. The memory map for this system is shown in Figure 2.



Instance	Base Address	High Address	Size
mb_opb			U
Ethernet_MAC	0x40c00000	0x40c0ffff	64K
dlmb_cntlr	0x00000000	0x00003fff	16K
ilmb_cntlr	0x00000000	0x00003fff	16K
LEDs_4Bit	0x40000000	0x4000ffff	64K
LED_7Segment1	0x40020000	0x4002ffff	64K
LED_7Segment2	0x40040000	0x4004ffff	64K
Push_Buttons_2Bit	0x40060000	0x4006ffff	64K
DIP_Switches_8Bit	0x40080000	0x4008ffff	64K
RS232	0x40600000	0x4060ffff	64K
USB_UART	0x40620000	0x4062ffff	64K
opb_intc_0	0x41200000	0x4120ffff	64K
debug_module	0x41400000	0x4140ffff	64K
opb_timer_1	0x41c00000	0x41c0ffff	64K
FLASH_2Mx16	0x21000000	0x213fffff	4M
DDR_SDRAM_16Mx16	0x22000000	0x23ffffff	32M

Figure 2 – BSB-generated Memory Map

3S1500MB Board Setup

The Memec Spartan-3 MB board should be configured as follows:

1. Uninstall all MODE jumper on J1.
2. Install a jumper on JP9 in the “BOARD” position (pins 1-2).
3. Install a jumper on JP10, pins 1-3.
4. Install two jumpers on JP8.
5. Install a jumper on JP7 in the “PROM ENABLE” position (pins 1-2).
6. Install a jumper on JP6 in the 3.3V position (pins 1-2).
7. No other jumpers should be installed.
8. Connect a straight through RS232 cable to the board DB-9 connector (JD1) and the serial port of the PC.
9. Connect an ethernet cable (either cross-over or straight-through will work) between the 3SMB board and either the PC or router.
10. Verify the Power switch (SW1) is in the OFF position.
11. Connect the AC/DC adapter to JP1.

Refer to Figure 3 for jumper locations.

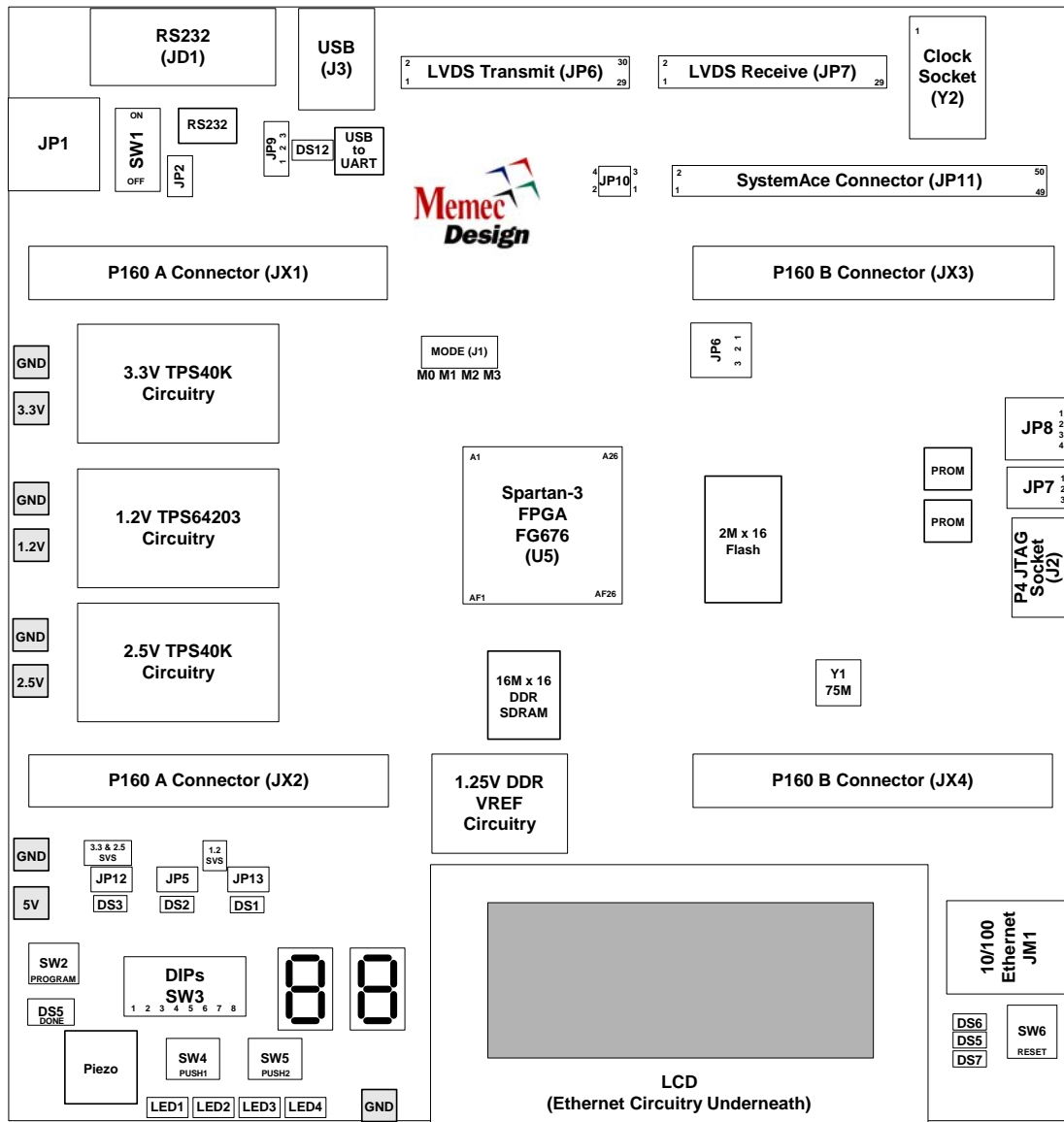


Figure 3 – Memec Spartan-3 MB Jumper Locations

Experiments

This example is based on the WebServer that Xilinx previously published in XAPP433 Version 1.0. The main differences are that this example runs on the 3SMB board and uses Internet Explorer.

The webserver source code is located in the /code directory. The LibXil Networking and File System libraries accessed by the webserver design are included by libgen.

The webserver is running HTTP 1.0 on this system; a file system (built using the LibXil Memory File System library) is used to store files. The server listens at port 8080 for requests. Every request is processed, and replies are served up by the server to the client.

Different demos are present in this system. These are:

- Hex Digit display in LEDs and 7-segment display – A hex digit selected in the web page, gets displayed as a 4 digit binary in LEDs and on 7-segment display DD1 on reload of the page
- Changing colors – Page background color changes on every reload of web pages
- DIP switches – Set the dip switches 1,2,3,4,5,6,7,8 and see it displayed as a binary value on reload of the page
- Browse to a second web page where the four LEDs can be individually turned ON or OFF

To compile and run this design, do the following:

1. Launch XPS.
2. Open the **system.xmp** project located at
.\Memec_3SMB_MicroBlaze_Basic\ 3SMB_WebServer_EDK81
3. Select the *Applications* tab.
4. Mark the software applications such that **Default: microblaze_0_bootloop** is the only thing marked for BRAM initialization, as shown in Figure 4.

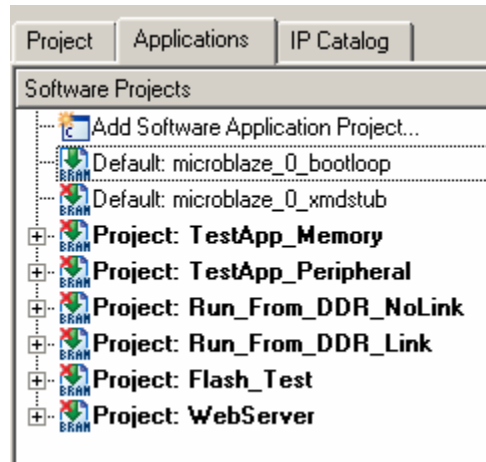


Figure 4 – WebServer Applications Tab

5. Double-click on source file `web.c` to open it in the editor.
6. Search in the source file for the command that initializes the device's IP address (`xilnet_ip_init`). Note the default IP address then close the file.
7. In XPS, select **Software** → **Software Platform Settings...**
8. With *Software Platform* selected, notice that the **xilnet** and **xilmfs** libraries have been selected for inclusion.

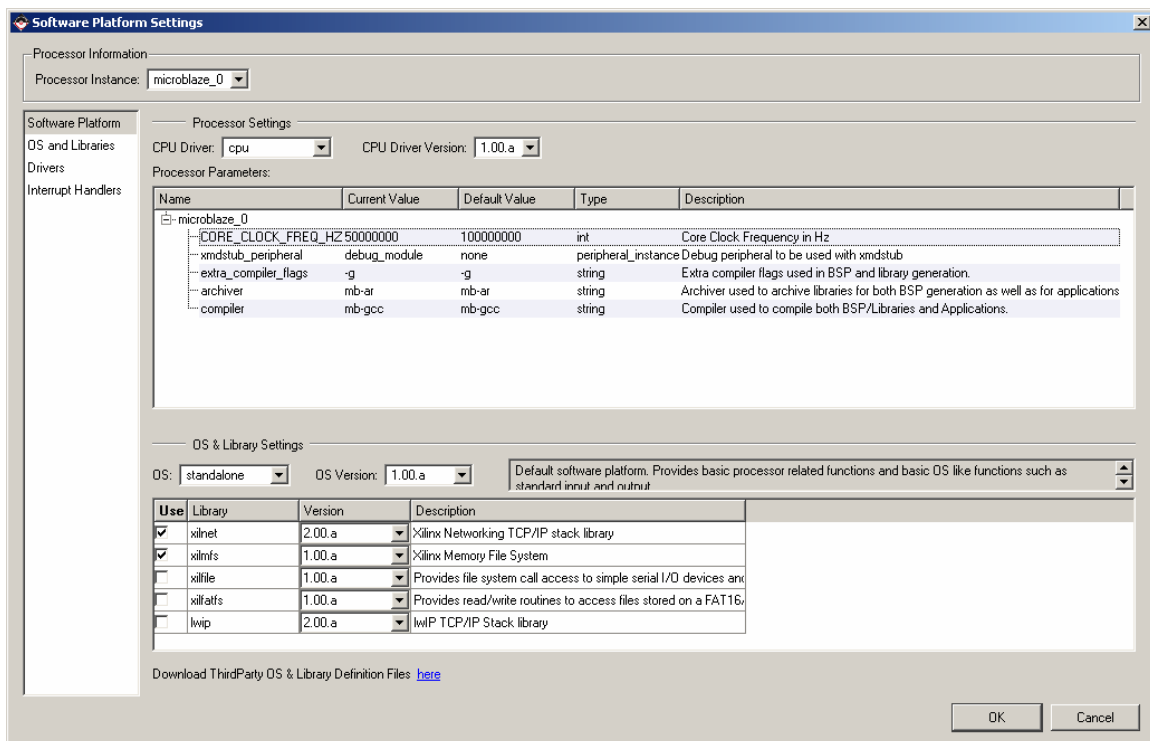


Figure 5 – Libraries to include in Software Platform

9. Now select *OS and Libraries*. Note that **xilnet** has *emac_instname* set to **Ethernet_MAC**, which is the opb_ethernet core. Also note that **xilmfs** parameter **base_address** has been assigned to 0x22010000, which falls in the address range of the DDR. This is the base address to which the embedded HTML files will be stored.

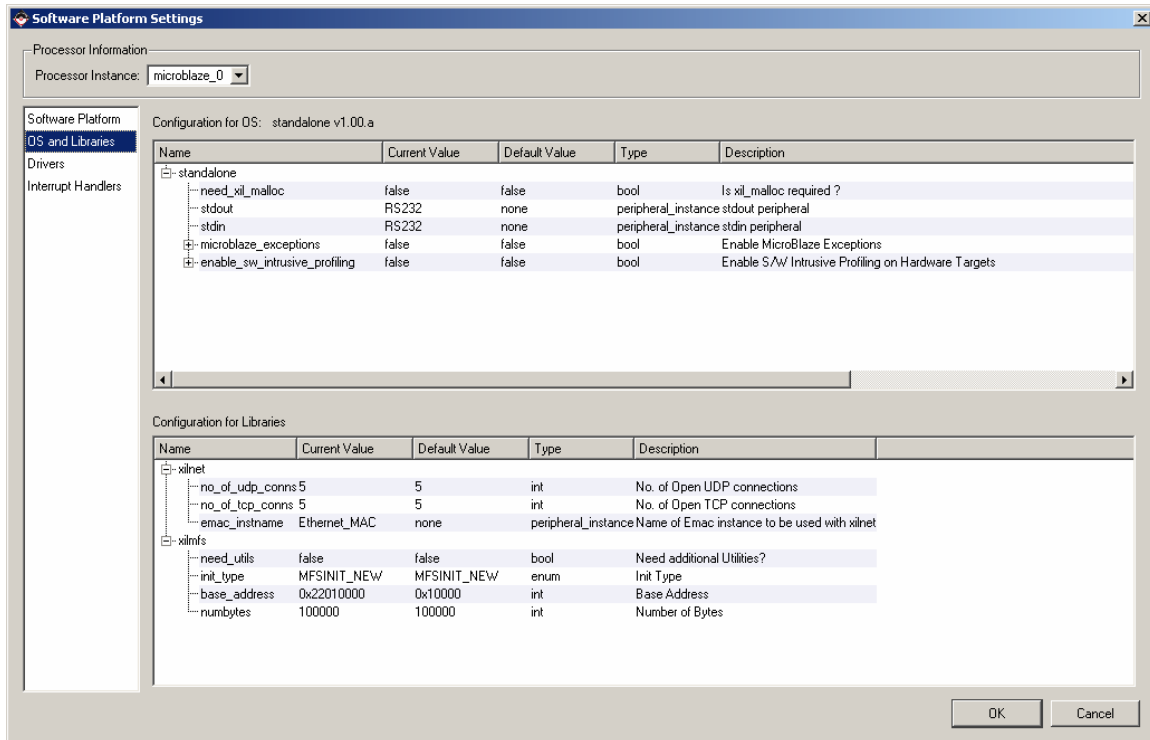


Figure 6 – Library/OS Parameters

10. Close the dialog by selecting **Cancel**.

To make a direct ethernet link between a PC and the 3SMB webserver, the IP addresses of the two devices must reside on the same subnet. As seen previously, the default IP address for the WebServer is 1.2.3.4. When the 3SMB is connected directly to the PC, the PC's IP address must be changed. If both the 3SMB and the PC are plugged into a router, then web.c can be modified to assign an IP to the WebServer that resides within the router's space.

To change the PC's IP address, do the following:

11. Launch Control Panel by selecting **Start → Settings → Control Panel**.
12. Double-click on **Network Connections**.
13. Right-click on **Local Area Connection** and select **Properties**.
14. Left-click once on **Internet Protocol (TCP/IP)** to select it, then click the **Properties** button.
15. Select the radio button for *Use the following IP address*:

16. Change the IP address to 1.2.3.9 and the Subnet mask to 255.0.0.0, as shown in

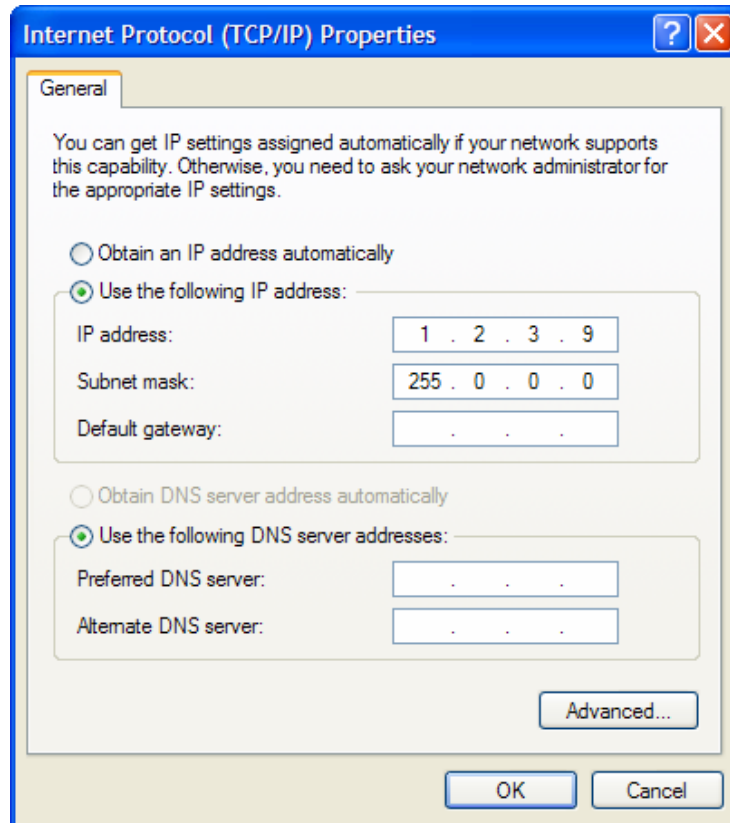


Figure 7 – Setting the PC's IP Address

17. Click **OK** to close the TCP/IP properties. Click **OK** again to close the Local Area Connection properties. The Network Connections window can be closed.

The demo is set up to run from DDR. For this reason, the bootloop is marked for BRAM initialization, and XMD will be used to boot-load the WebServer code to DDR and run it. To run the demo, do the following:

18. Turn power on to the board.
19. Select **Device Configuration → Download Bitstream**.
20. In the *Applications* tab, right-click on **Project: WebServer** and select **Build Project**.
21. Open a HyperTerminal with settings of 115200, 8, N, 1, N.
22. Launch XMD. Type the following commands in XMD to download the WebServer code to the DDR (over an accelerated FSL download link that is present in the hardware) and then begins executing the code in DDR (see Figure 8).

```
dow webserver/executable.elf
con
```

```
C:\EDK81\bin\nt\xmd.exe
<0x22000000-0x23ffffff> DDR_SDRAM_16Mx16 dxc1
<0x40000000-0x4000ffff> LEDs_4Bit mb_opb
<0x40020000-0x4002ffff> LED_7Segment1 mb_opb
<0x40040000-0x4004ffff> LED_7Segment2 mb_opb
<0x40060000-0x4006ffff> Push_Buttons_2Bit mb_opb
<0x40080000-0x4008ffff> DIP_Switches_8Bit mb_opb
<0x40600000-0x4060ffff> RS232 mb_opb
<0x40620000-0x4062ffff> USB_UART mb_opb
<0x40c00000-0x40c0ffff> Ethernet_MAC mb_opb
<0x41200000-0x4120ffff> opb_intc_0 mb_opb
<0x41400000-0x4140ffff> debug_module mb_opb
<0x41c00000-0x41c0ffff> opb_timer_1 mb_opb

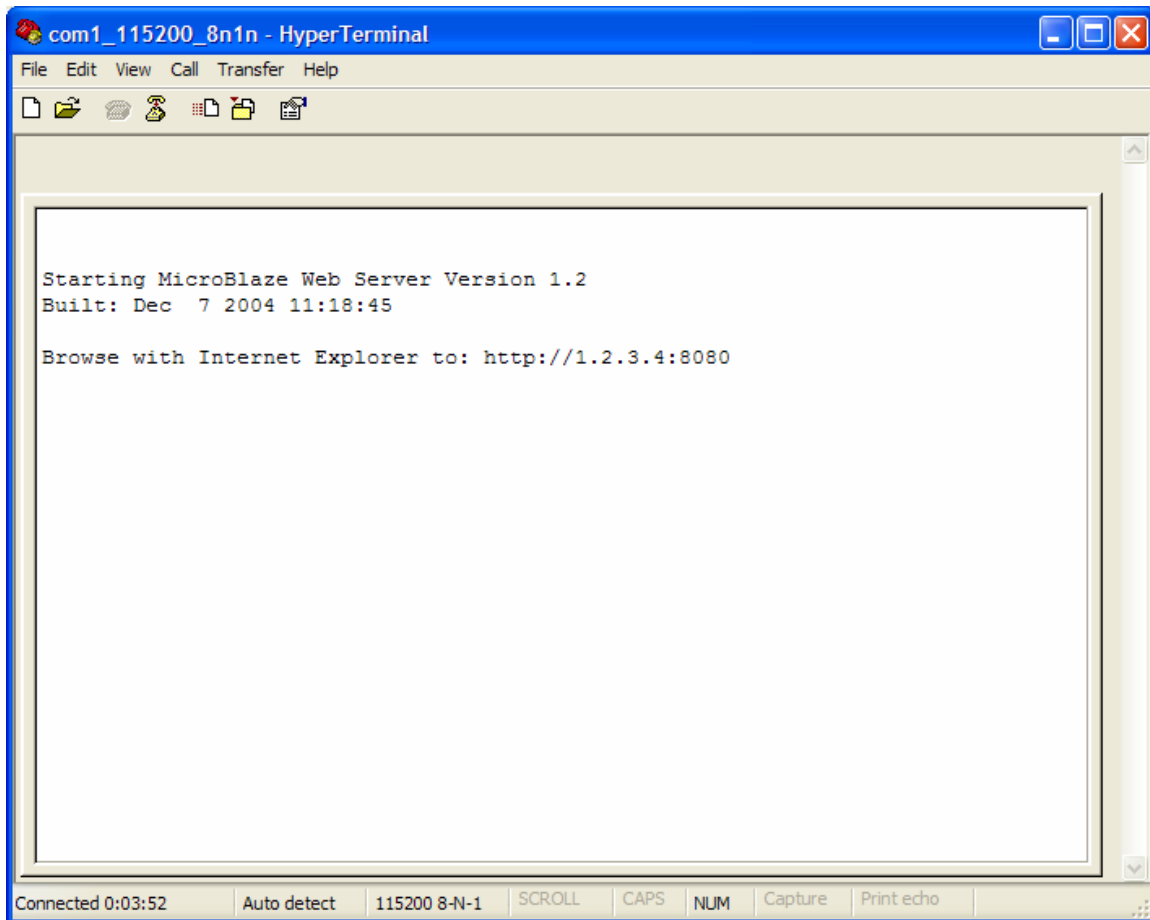
Connecting to cable <Parallel Port - LPT1>.
Checking cable driver.
Driver windrvr6.sys version = 7.0.0.0. LPT base address = 0378h.
ECP base address = 0778h.
ECP hardware is detected.
Cable connection established.
Connecting to cable <Parallel Port - LPT1> in ECP mode.
Checking cable driver.
Driver xpc4drv.sys version = 1.0.4.0. LPT base address = 0378h.
Cable Type = 1, Revision = 3.
Setting cable speed to 5 MHz.
Cable connection established.

JTAG chain configuration
-----
Device ID Code IR Length Part Name
1 05046093 8 XCF04S
2 05044093 8 XCF01S
3 01434093 6 XC3S1500
Assuming Device No: 3 contains the MicroBlaze system
Connected to the JTAG MicroProcessor Debug Module (MDM)
No of processors = 1

MicroBlaze Processor 1 Configuration :
-----
Version.....4.00.a
No of PC Breakpoints.....2
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....on
Instruction Cache Base Address.....0x22000000
Instruction Cache High Address.....0x23ffffff
Data Cache Support.....on
Data Cache Base Address.....0x22000000
Data Cache High Address.....0x23ffffff
Exceptions Support.....off
FPU Support.....off
FSL DCache Support.....on
FSL ICache Support.....on
Hard Divider Support.....off
Hard Multiplier Support.....on
Barrel Shifter Support.....off
MSR clr/set Instruction Support....off
Compare Instruction Support.....off
Number of FSL ports.....1
MBsfsl(0)-MDMfsl(0) Connected.....Yes
JTAG MDM Connected to MicroBlaze 1
Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD% dow webserver/executable.elf
section, .vectors.reset: 0x00000000-0x00000008
section, .vectors.sw_exception: 0x00000008-0x00000010
section, .vectors.interrupt: 0x00000010-0x00000018
section, .vectors.hw_exception: 0x00000020-0x00000028
section, .text: 0x22000000-0x22006618
section, .init: 0x22006618-0x22006644
section, .fini: 0x22006644-0x22006664
section, .ctors: 0x22006664-0x2200666c
section, .dtors: 0x2200666c-0x22006674
section, .rodata: 0x22006674-0x2200764a
section, .data: 0x22007650-0x22007a3c
section, .jcr: 0x22007a3c-0x22007a40
section, .bss: 0x22007a40-0x22008dc8
Downloaded Program webserver/executable.elf
Setting PC with program start addr = 0x00000000
XMD% con
Processor started. Type "stop" to stop processor
RUNNING>
```

Figure 8 – XMD Launched

23. A proper download and launch of the code will give the results in HyperTerminal shown in Figure 9.



```
com1_115200_8n1n - HyperTerminal
File Edit View Call Transfer Help

Starting MicroBlaze Web Server Version 1.2
Built: Dec 7 2004 11:18:45

Browse with Internet Explorer to: http://1.2.3.4:8080

Connected 0:03:52 Auto detect 115200 8-N-1 SCROLL CAPS NUM Capture Print echo
```

Figure 9 – UART Output from WebServer Design

24. Launch a browser and point it to <http://1.2.3.4:8080> (see Figure 10) (If you changed the IP address in web.c, this will be displayed in HyperTerminal. Point to <http://x.x.x.x:8080>, where x.x.x.x is the IP address you specified for the web server.) Note that you must explicitly type in the <http://> prefix and the “:8080” port in order for this to work.



Figure 10 – Internet Explorer Displaying 3SMB Page

At this point, selecting a hex number in the **Hex Value** field and clicking **Submit** will light the LEDs and display that value on 7-segment display DD1. For example hex number 'A' (binary 1010) will light LED1 and LED3 and display character 'A' on DD1.

Also, changing the DIP Switches and then hitting **Submit** will change the **DIP Value** that is readback. Every time the **Submit** button is pressed, the background color will change.

Pressing the HyperLink for **Click here to Control LEDs individually** shows a second web page stored on the 3SMB board, which is shown in Figure 11.

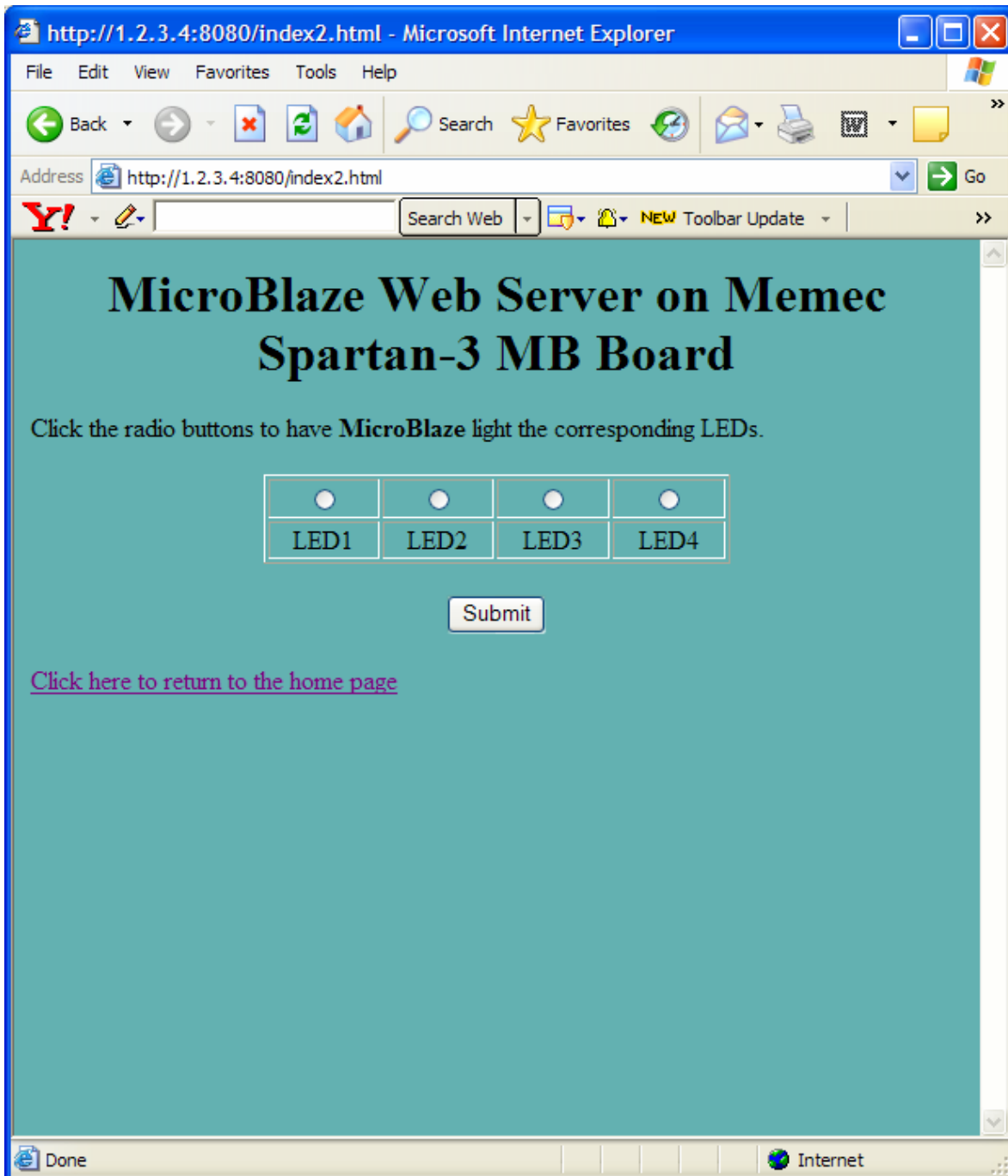


Figure 11 – index2.html on 3SMB MicroBlaze

Optional BootLoader Exercise

The WebServer application can be stored in flash and executed from a bootloader. To do this, follow the instructions in document *Memec 3SMB MicroBlaze Using Memory Reference Designs*, Section *Bootloader*.

Revision History

Date	Version	Revision
12/07/04	6.3	Initial Memec release.
12/21/04	6.3a	Updated to new BSB design; added bootloader pointer
09/29/05	7.1	Updated to EDK 7.1
07/07/06	8.1	Updated to EDK 8.1; Added CacheLink and asynchronous DDR operation; Adding BCM5221 code to force 10Mbps operation. (bhf)