Memec 3SMB MicroBlaze Piezo Reference Design

July 10, 2006
Version 8.1

Overview

This document describes a simple reference design that uses the Xilinx MicroBlaze™ soft processor core to exercise a piezo audio transducer on the Memec Spartan-3 MB development board. Along with the piezo interface, this design also has a uart peripheral core to provide a simple RS232 interface to the UART device located on the Memec Spartan-3 MB MicroBlaze development board.

Experiment Setup

Software

The recommended software setup for this reference design is:

- Windows2000 or WindowsXP
- Xilinx ISE 8.1i (Foundation or BaseX) with latest Service Pack[1]
- Xilinx EDK 8.1 with latest Service Pack[1]

Hardware

The hardware setup used by this reference design includes:

- Computer with a recommended minimum of 1GB RAM and 1 GB Virtual Memory[2]
- Memec Spartan-3 MB Development Kit
- Platform USB Cable or JTAG Programming Cable IV
- Serial Cable

[1] Latest Service Packs are available at www.support.xilinx.com/swupdate
[2] Refer to the *ISE 8.1i Release Notes and Installation Guide* http://toolbox.xilinx.com/docsan/xilinx8/books/docs/irn/irn.pdf

Block Diagram

The following figure shows a high-level block diagram for this reference design.

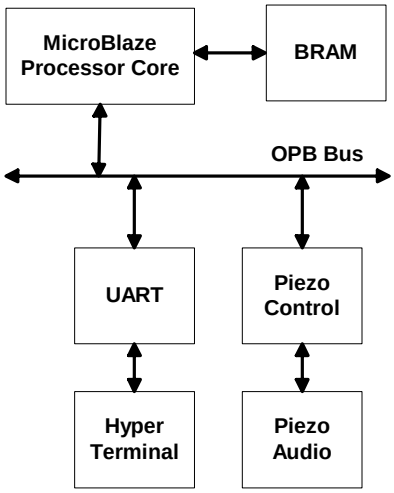

Figure 1 - Hello World Design

Memory Map

The MicroBlaze processor provides 4G of address space that can be used to access memory and I/O devices that reside on the processor bus. For this reference design, the UART, piezo controller, and the processor memory are memory mapped as shown in Figure 2.

Instance	Prefix	Base Address	High Address	Size	Min Size
memec_piezo_0		0xFFFF9000	0xFFFF9003	4	0x04
memec_piezo_0	mir	0xFFFF9004	0xFFFF9007	4	0x04
myuart		0xFFFF_8100	0xFFFF_81FF	256	0x100
my_dopb				UNSPECIFIED	0x200
lmb_bram_if_cntlr_0		0x0000_0000	0x0000_3FFF	16 KB	0x800
lmb_bram_if_cntlr_1		0x0000_0000	0x0000_3FFF	16 KB	0x800

Figure 2 - Design Memory Map

Data and Code Memory

The data and code for this application will reside in the on-chip BLOCKRAM. The Spartan-3 MB MicroBlaze development board is designed with the XC3S1500-4FG676C Xilinx FPGA. The XC3S1500 contains 32 BLOCKRAMs at 2Kbytes per block. A XC3S1500 MicroBlaze design can have a maximum of 64Kbytes on-chip processor

memory. This reference design uses 8 BLOCKRAMs to provide 16Kbytes of memory to the processor.

UART Port

The UART port for this reference design is used to interface to the HyperTerminal. The application uses STDOUT to print a welcome banner to the RS232 port.

Piezo Audio Transducer

The 3SMB board is designed with an FPGA I/O signal interfaced to a piezo audio transducer. A clock signal in the audio frequency range sent to the piezo from the FPGA will produce a sound with that frequency. The piezo controller peripheral included in this design provides an OPB interface where an 8-bit number can be used to derive a specific frequency and sound.

The formula for calculating the resulting frequency based on the 8-bit input is as follows:

Piezo Frequency = (OPB Frequency) / (INPUT * 1024)

For example, this design's OPB runs at 75 MHz. For an INPUT of 0x24, the resulting frequency is calculated as follows:

Piezo Frequency = (75 MHz) / (0x24 * 1024)
Piezo Frequency = (75 MHz) / (36864) = 2035 Hz

3S1500MB Board Setup

The Memec Spartan-3 MB board should be configured as follows:

1. Uninstall all MODE jumper on J1.
2. Install a jumper on JP9 in the "BOARD" position (pins 1-2).
3. Install a jumper on JP10, pins 1-3.
4. Install two jumpers on JP8.
5. Install a jumper on JP7 in the "PROM ENABLE" position (pins 1-2).
6. Install a jumper on JP6 in the 3.3V position (pins 1-2).
7. No other jumpers should be installed.
8. Connect a straight through RS232 cable to the board DB-9 connector (JD1) and the serial port of the PC.
9. Verify the Power switch (SW1) is in the OFF position.
10. Connect the AC/DC adapter to JP1.

Refer to Figure 3 for jumper locations.

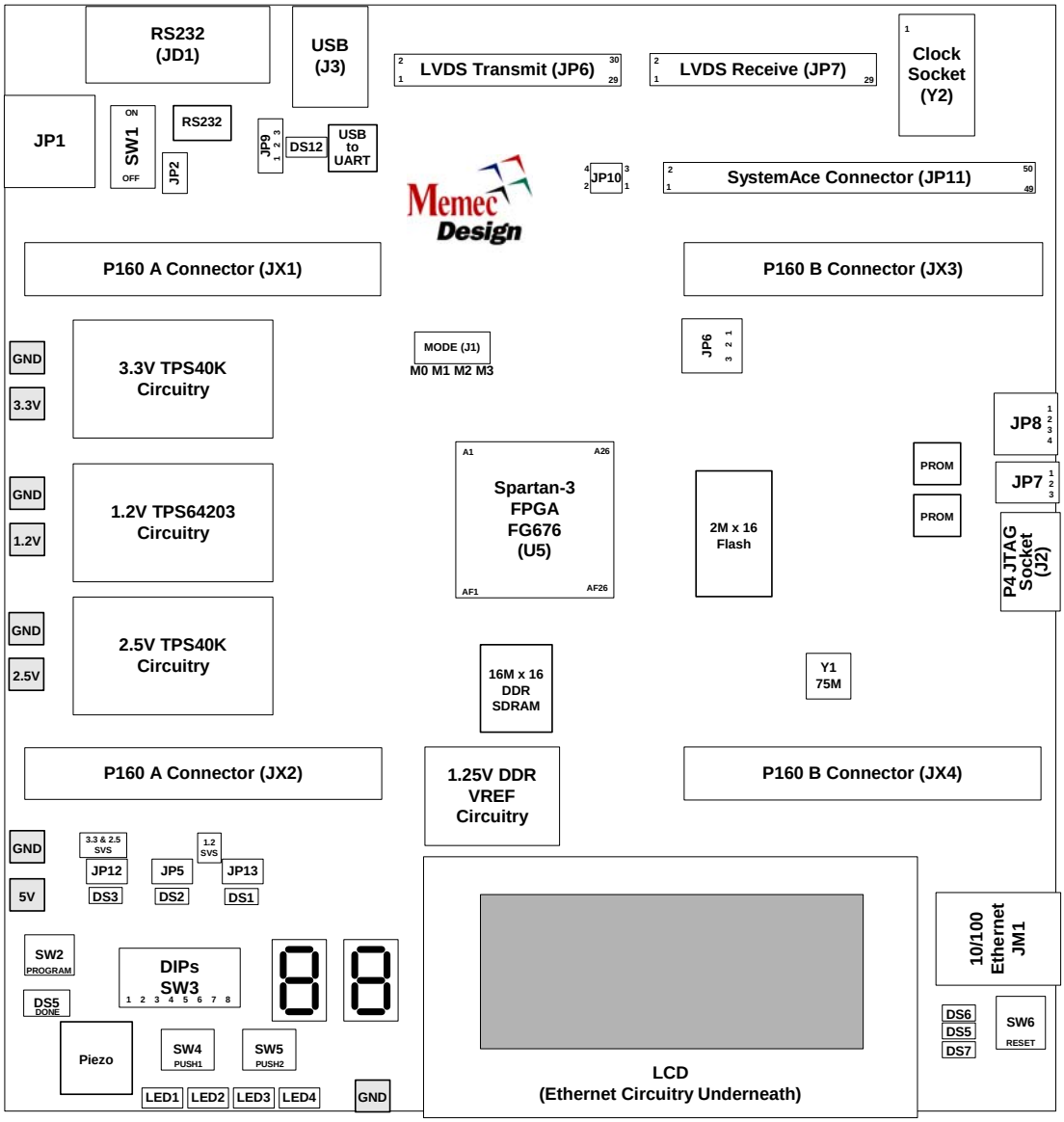

Figure 3 – Memec Spartan-3 MB Jumper Locations

Experiments

This reference design provides three different audio sequences as examples. The application first prints a welcome banner to the RS232 UART. Then two short audio sequences are played. The third audio sequence is a simple scale from 0x01 to 0xFF, which repeats endlessly.

This example uses a 19200 HyperTerminal for RS232 UART output. Refer to Appendix A: Starting a HyperTerminal Session section for instructions on starting the

HyperTerminal, or simply click the shortcut **com1_19200_8n1n.ht** provided with the reference designs.

Implementing the Project to Create a Bitstream

1. Start XPS and select **File→Open Project**
2. Browse to `Memec_3SMB_MicroBlaze_Basic\3SMB_Piezo_EDK81`. Select system.xmp, and select **Open**. You should see the following XPS GUI.

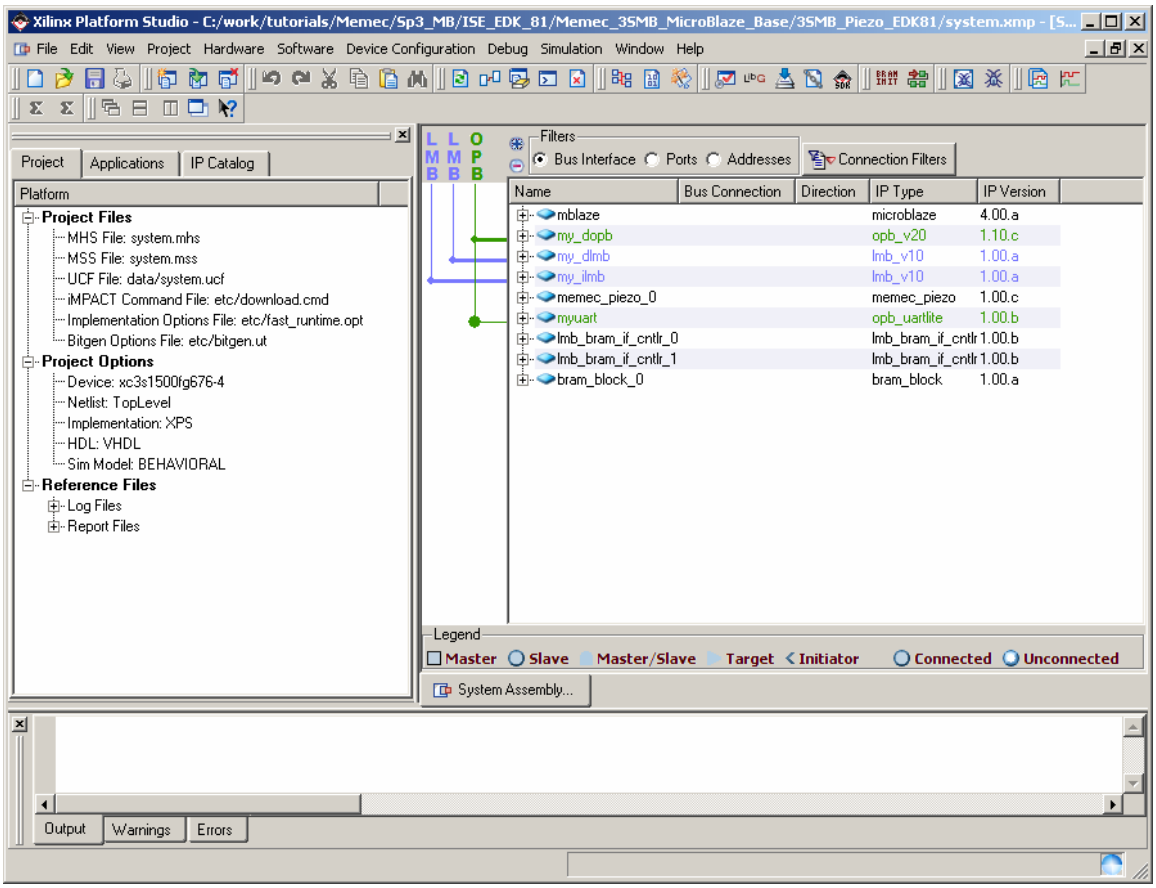

Figure 4 – Piezo Project Open in XPS

3. Switch to the Applications tab. Expand the Sources under **Project: Piezo_Songmaker**. Double-click on system.c to open the C source code in the editor window. Review the code for the design.
4. Generate libraries (**Tools→Generate Libraries and BSPs**)
5. Compile program sources (**Tools → Build All User Applications**)
6. Generate Netlist (**Tools→Generate Netlist**)
7. Generate Bitstream (**Tools→Generate Bitstream**)
8. Update the bitstream with the program (**Tools→Update Bitstream**)

Running The Application Program

1. Slide the power switch to the ON position.

2. Verify the three power LEDs labeled 1.2V (DS2), 2.5V (DS1), and 3.3V (DS6) turn on.
3. Go to the XPS GUI and download the bitstream into the FPGA (**Device Configuration → Download**). Upon completion of the download, you should see the following on the HyperTerminal.

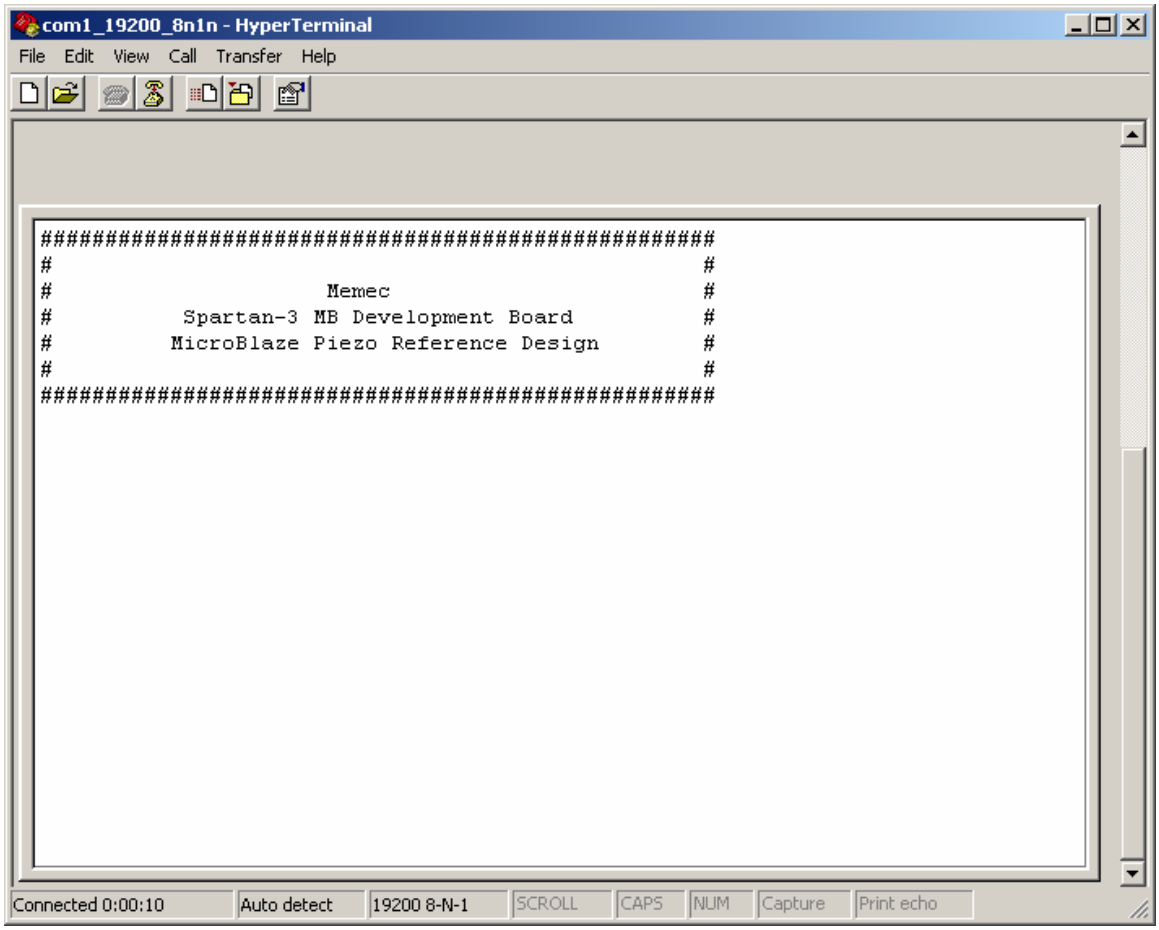

Figure 5 – RS232 Output from Piezo Project

Revision History

Date	Version	Revision
12/07/04	6.3	Initial Memec release at EDK 6.3
09/28/05	7.1	Update to EDK 7.1
07/10/06	8.1	Update to EDK 8.1

Appendix A: Starting a HyperTerminal Session

1. Start a HyperTerminal session (**Start→Programs→Accessories→Communications→HyperTerminal**).

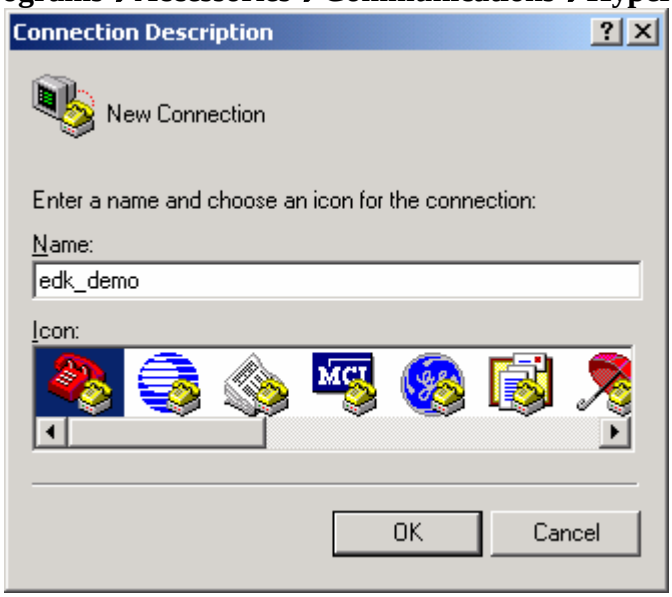

Figure 6 – HyperTerminal Connection Name

2. Enter edk_demo in the "Name" field and select OK.

Figure 7 – HyperTerminal COM

3. Select "COM1" from "Connect using" drop down menu and select OK.

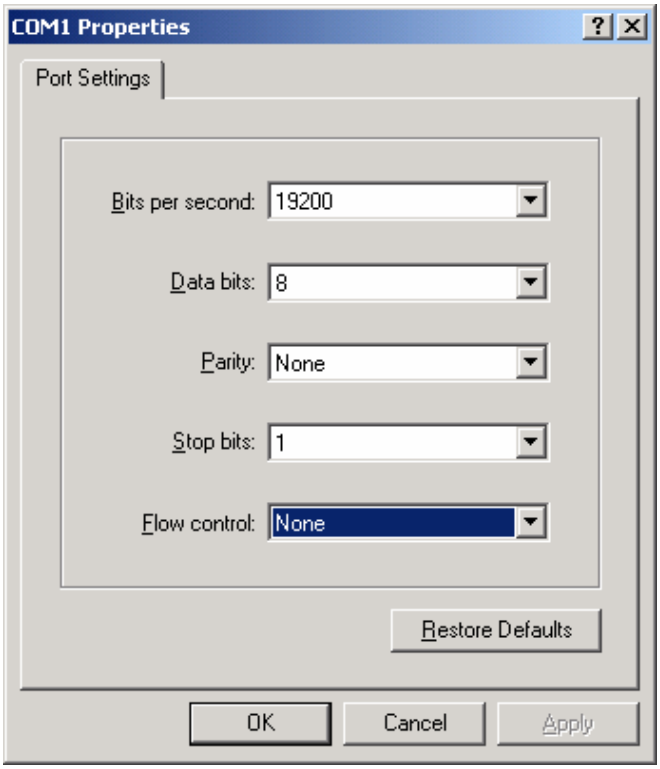

Figure 8 – HyperTerminal Settings

4. Enter the above port settings and then select OK. You should see the following HyperTerminal window.

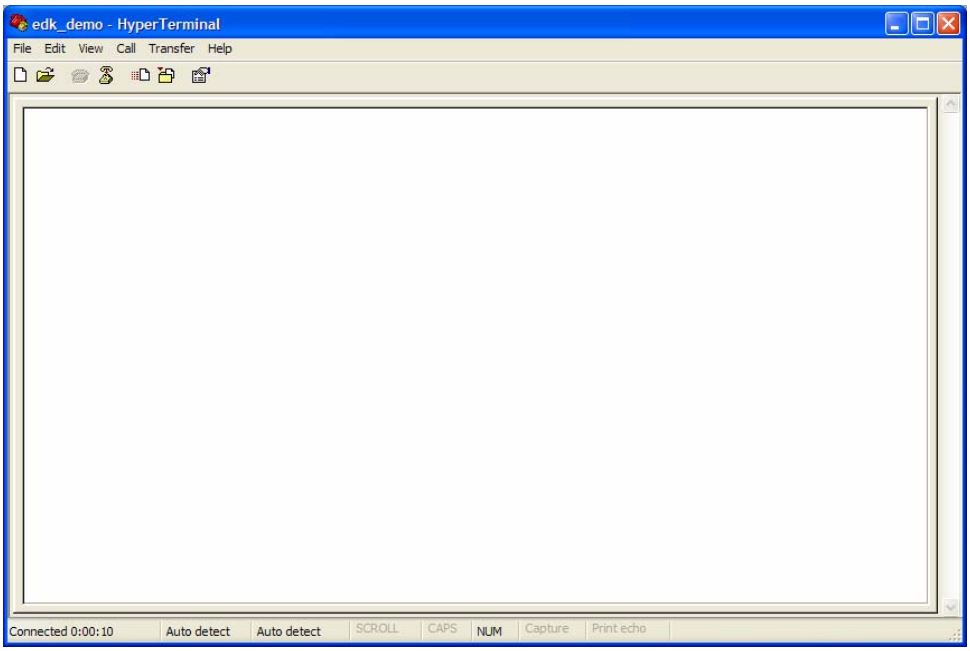

Figure 9 – HyperTerminal Launched