Memec Spartan-3 MB User's Guide

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Version 2.2

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Overview

The Spartan-3 MB Development Kit provides a complete, low cost solution for developing designs and applications based on the Xilinx Spartan-3 FPGA family. The kit bundles a full-featured, expandable Spartan-3 based system board with a power supply, user's guide, and reference designs. Optional Xilinx software and P160 application specific expansion modules are also available.

The Spartan-3 MB system board utilizes the 1.5 million-gate Xilinx Spartan-3 device (XC3S1500-4FG676) in the 676-pin fine-grid array package. The high gate density and advanced features included in the Spartan-3 FPGA allows complete system solutions to be implemented in the low cost device. The system board includes an abundance of on-board features that simplify system prototyping and proof of concept projects. Both DDR and flash memory are included for processor systems and DSP applications. External interfaces support USB, 10/100 Ethernet, serial, and LVDS. Two P160 expansion module slots are available to easily add application specific daughter cards. User switches, LEDs, 7-segment LEDs, and a 2 x 16 Character LCD are also included. Configuration through JTAG, Platform Flash Proms, and an optional System ACE interface round out the system design.

The Spartan-3 FPGA family has the advanced features needed to fit the most demanding, high volume applications. The Memec Design Spartan-3 MB Development Kit provides a feature-rich platform to explore the most demanding applications, allowing you to quickly and effectively meet your time-to-market requirements.

Spartan-3 MB Development Board

A photograph of the Spartan-3 MB development board is shown in Figure 1. Various features and circuits are pointed out. A diagram is shown in Figure 2 which shows the reference designators for all of the jumpers discussed in this User's Guide.

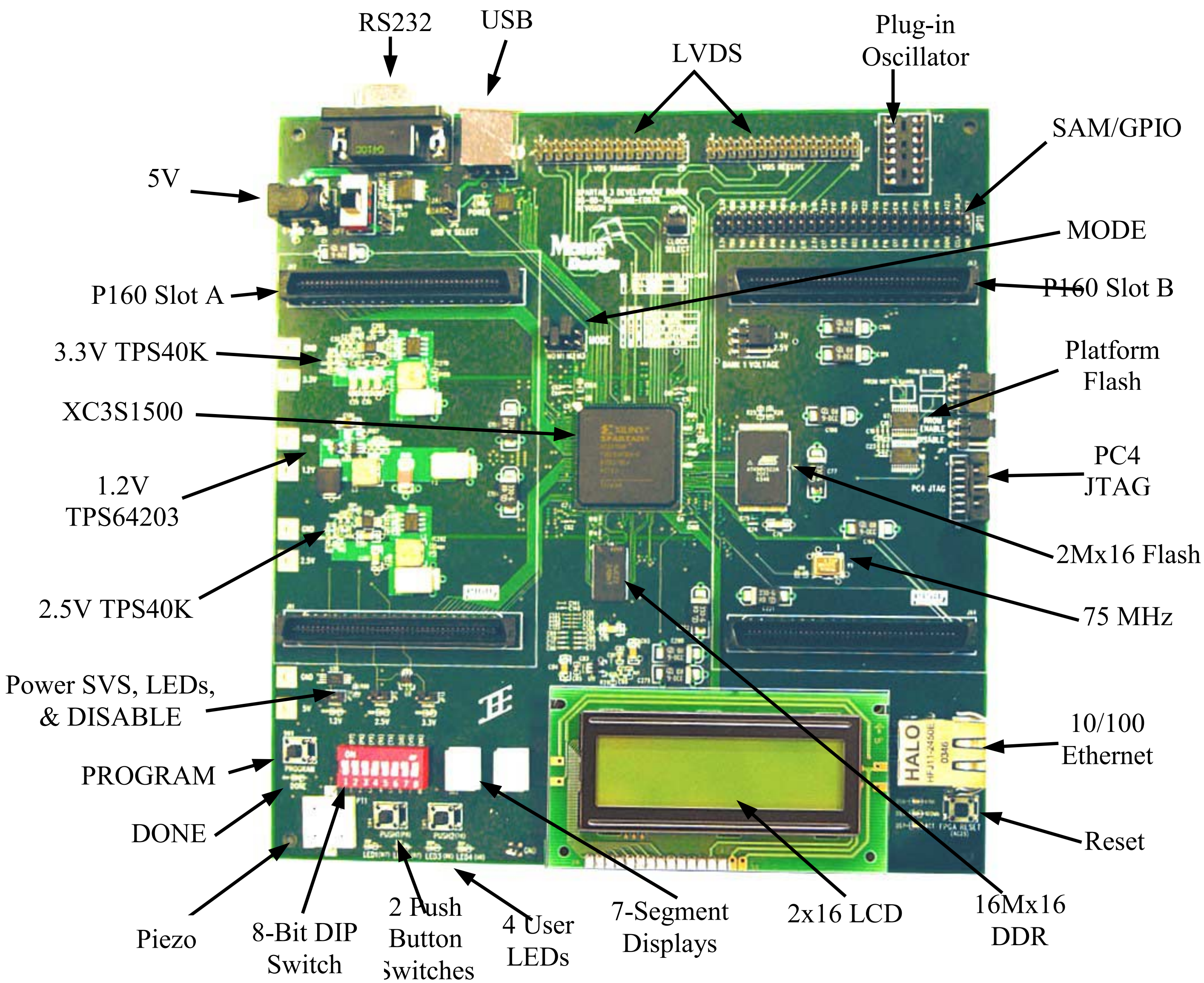

Figure 1 – Spartan-3 MB Development Board

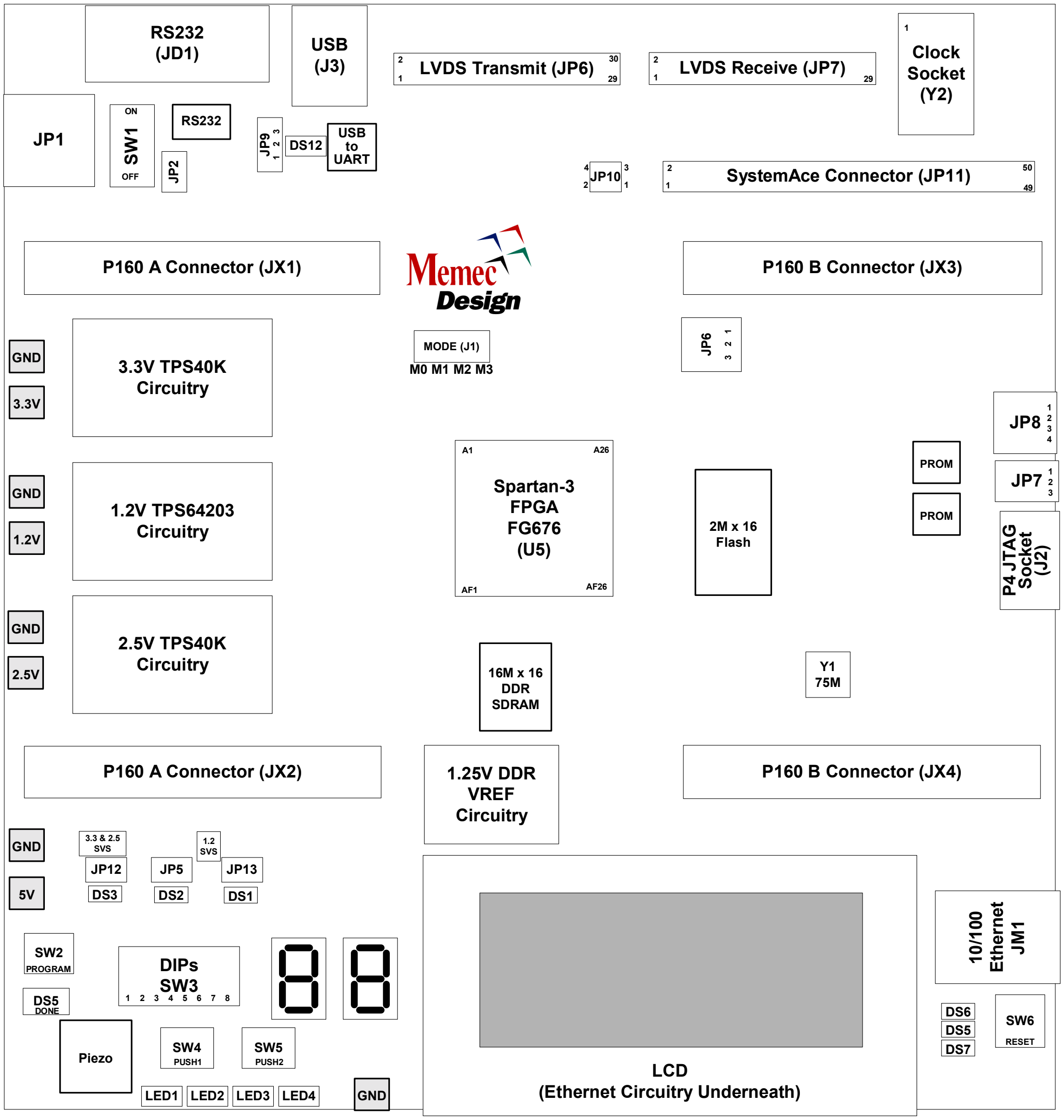

Figure 2 – Spartan-3 MB Development Board Jumpers

Spartan-3 MB Development Board Block Diagram

A high-level block diagram of the Spartan-3 MB development board is shown in Figure 3 followed by a description of each board sub-section. Each section lists the applicable pin connections for that device; this information is also included in a master User Constraint File (UCF) included on the CD.

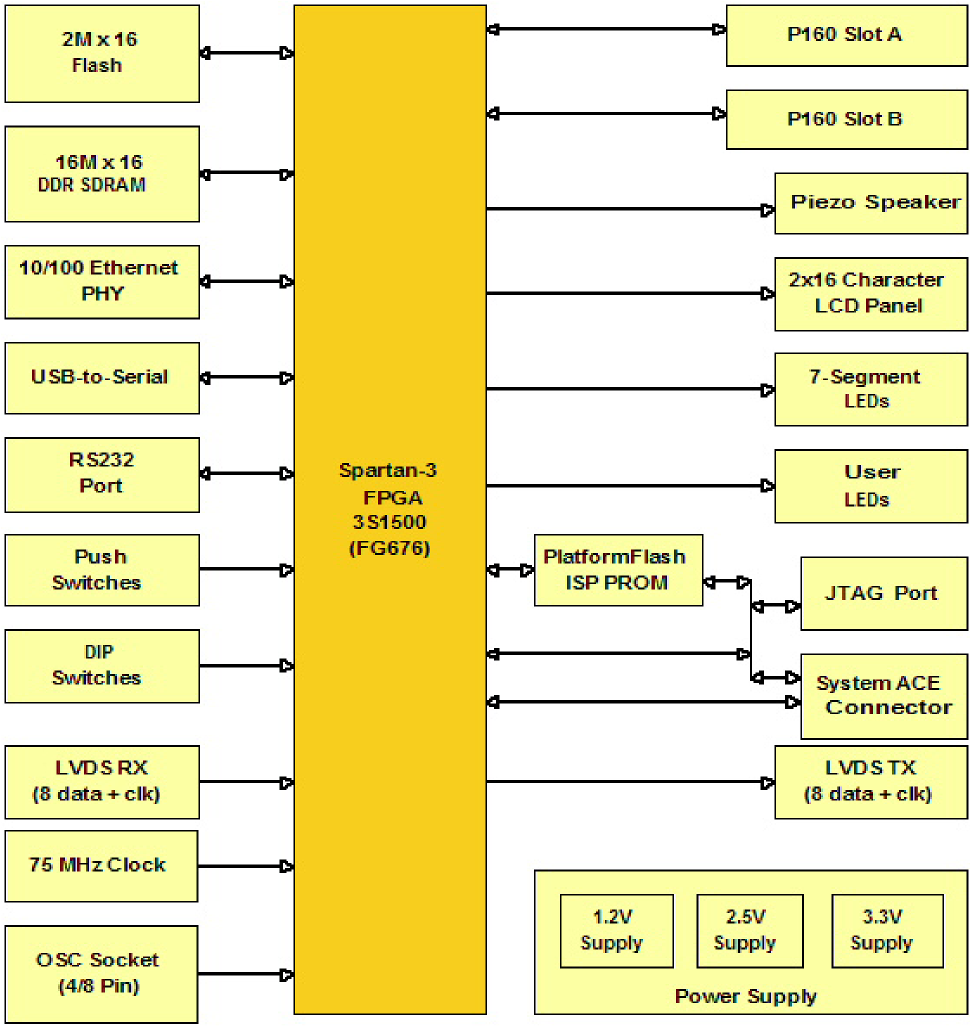

Figure 3 – Spartan-3 MB Block Diagram

Spartan-3 Device

The Spartan-3 MB development board utilizes the Xilinx XC3S1500-4FG676C FPGA. This devices offers 1.5M gates of flexible design space. The 1.2V Spartan-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50K to 5M system gates.

The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logic resources, the total number of I/Os, and the overall level of performance. Numerous additional enhancements are inherited from state-of-the-art Virtex-II technology, including 18Kb internal BlockRAMs, embedded 18x18 hardware multipliers, enhanced I/O (such as DCI, DDR registers, and additional I/O standards), and advanced clock management functions (like frequency synthesis and phase-shifting). These Spartan-3 enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment. The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Clock Generation

A 2.5V, 75 MHz, surface-mount Pletronics oscillator provides the primary clock source for the Spartan-3 MB development board (signal name CLK_SMT, Y1.3). The Pletronics SM7745HV and SM7745DV oscillator families offer pin-compatible alternatives with frequencies ranging from 1.5 MHz to 170 MHz.

The Spartan-3 MB development board also provides an on-board 14-pin socket which can accommodate a user-supplied, half- or full-can, 3.3V oscillator (signal name CLK_SOCKET, Y2.8 or Y2.11). The Pletronics SQ3345V and SQ3345VW oscillator families fit this socket, offering frequencies ranging from 650 KHz to 170 MHz.

If a SystemACE Module (SAM) is connected to JP11, the SAM clock is also available to the FPGA (either as an input or output, depending on SAM JP5). On the 3SMB, either the SAM clock (JP11.6) or CLK_SOCKET can be selected for connection to the FPGA through signal FPGA_GCLK. If CLK_SOCKET is selected as the source for the SAM, the plug-in oscillator (Y2) frequency must be less than 33 MHz due to the SystemACE controller. The selection for the clock routing for FPGA_GCLK and the SAM clock is based on the setting of header JP10, as described in Table 1.

Table 1 – JP10 Configuration

3SMB JP10 Connection	SAM JP5 Connection	FPGA_GCLK Source	SAM Clock Source
1-2, 3-4	Closed	CLK_SOCKET	CLK_SOCKET
1-3	Open	SAM 25 MHz Clock	SAM 25 MHz Clock

The FPGA clock pin-out is shown in Table 2.

Table 2 – Spartan-3 MB Board Clocks

Signal Name	Spartan-3 Pin #	Direction	Description
CLK_SMT	AE14	Input	75MHz oscillator
FPGA_GCLK	A13	Input	3.3V oscillator socket or SAM clock

User Interfaces

For simple feedback and user interaction, the Spartan-3 MB development board provides several user interfaces, described in the following sections:

User 7-Segment LED Displays

The Spartan-3 MB development board utilizes two common-anode 7-segment LED displays that can be used during the test and debugging phase of a design. The user can turn a given segment ON by driving the associated signal low. The I/O standard can be set to either 3.3V LVCMOS or 3.3V LVTTL. Figure 4 shows the user 7-segment display interface to the Spartan-3 FPGA.

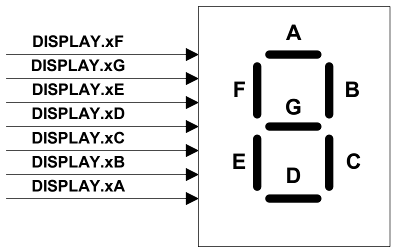

Figure 4 – 7-Segment LED Display Interface

Table 3 shows the 7-Segment LED display pin descriptions.

Table 3 – 7-Segment Display Signal Descriptions (DD1 & DD2)

Signal Name	Spartan-3 Pin #	Direction	Description
DISPLAY.1A	AC17	Output	7-Segment LED Display DD1, Segment A
DISPLAY.1B	AB17	Output	7-Segment LED Display DD1, Segment B
DISPLAY.1C	AA16	Output	7-Segment LED Display DD1, Segment C
DISPLAY.1D	AB16	Output	7-Segment LED Display DD1, Segment D
DISPLAY.1E	AC16	Output	7-Segment LED Display DD1, Segment E
DISPLAY.1F	AF20	Output	7-Segment LED Display DD1, Segment F
DISPLAY.1G	AE20	Output	7-Segment LED Display DD1, Segment G
DISPLAY.2A	AA14	Output	7-Segment LED Display DD2, Segment A
DISPLAY.2B	Y14	Output	7-Segment LED Display DD2, Segment B
DISPLAY.2C	AD15	Output	7-Segment LED Display DD2, Segment C
DISPLAY.2D	AB15	Output	7-Segment LED Display DD2, Segment D
DISPLAY.2E	AA15	Output	7-Segment LED Display DD2, Segment E
DISPLAY.2F	W14	Output	7-Segment LED Display DD2, Segment F
DISPLAY.2G	AD14	Output	7-Segment LED Display DD2, Segment G

User LEDs

The Spartan-3 MB development board provides four user LEDs, as shown in Table 4. The I/O standard is 3.3V LVCMOS or 3.3V LVTTL.

Table 4 – User LED Signal Descriptions (DS3, DS4, DS7, DS8)

Signal Name	Spartan-3 Pin #	Direction	Description
LED1	W7	Output	LED is ON when signal is low
LED2	R7	Output	LED is ON when signal is low
LED3	R6	Output	LED is ON when signal is low
LED4	U6	Output	LED is ON when signal is low

User Push Buttons

The Spartan-3 MB development board design provides three user push button switch inputs to the Spartan-3 FPGA. Each push button switch can be used to generate an active low signal. Push button SW6 is labeled to be a RESET signal into the FPGA. Pushing a push button connects the node to Ground (logic low). Internal Spartan-3 pull-ups must be used to force a logic high when the push button is not pushed. The I/O standard is 3.3V LVCMOS or 3.3V LVTTL.

A pinout and description of the push buttons are shown in Table 5.

Table 5 – User Push Button Signal Descriptions (SW4, SW5, SW6)

Signal Name	Spartan-3 Pin #	Direction	Description
PUSH1	P8	Input	User Push Button Switch Input 1 (SW4)
PUSH2	T6	Input	User Push Button Switch Input 2 (SW5)
PUSH_RESET	AC25	Input	User Push Button Switch Reset (SW6)

User DIP Switch

The Spartan-3 MB development board provides eight user DIP switch inputs. These switches can be statically set to a low or high logic level. When the switch is disconnected from Ground (logic low), internal Spartan-3 pull-ups are required to generate a logic high. The I/O standard is 3.3V LVCMOS or 3.3V LVTTL.

A diagram of the User DIP switch interface is shown in Figure 5.

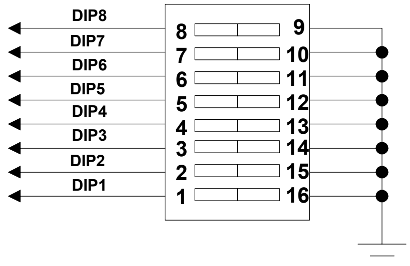

Figure 5 – User DIP Switch Interface (SW3)

A pinout and description are shown in Table 6.

Table 6 – User DIP Switch Signal Descriptions (SW3)

Signal Name	Spartan-3 Pin #	Direction	Description
DIP1	P7	Input	User Switch Input 1
DIP2	P6	Input	User Switch Input 2
DIP3	P5	Input	User Switch Input 3
DIP4	R5	Input	User Switch Input 4
DIP5	T5	Input	User Switch Input 5
DIP6	U5	Input	User Switch Input 6
DIP7	V5	Input	User Switch Input 7
DIP8	W6	Input	User Switch Input 8

LCD Module

The Spartan-3 MB system board provides an 8-bit interface to a 2x16 LCD panel. The following table shows the LCD interface signals.

Table 7 – LCD Interface Signal Description

Signal Name	Spartan-3 Pin #	Description
D0	W5	LCD Data Bit 0
D1	W3	LCD Data Bit 1
D2	V7	LCD Data Bit 2
D3	U7	LCD Data Bit 3
D4	T7	LCD Data Bit 4
D5	T8	LCD Data Bit 5
D6	R8	LCD Data Bit 6
D7	V6	LCD Data Bit 7
EN	AB3	LCD Enable Signal
RS	AB4	LCD Register Select Signal
RW		LCD Write Signal (this signal is connected to logic "0" on the Spartan-3 MB system board).

RS232 Port

The Spartan-3 MB development board provides an RS232 port that can be driven by the Spartan-3 FPGA. A subset of the RS232 signals are used on the Spartan-3 development board to implement this interface (RD and TD signals).

The Spartan-3 MB development board provides a DB-9 connection for a simple RS232 port. This board utilizes the Texas Instruments MAX3221 RS232 driver for driving the RD and TD signals. The user provides the RS232 UART code, which resides in the Spartan-3 FPGA.

A diagram of the RS232 interface is shown in Figure 6. Table 8 shows the RS232 signals and their pin assignments to the Spartan-3 FPGA.

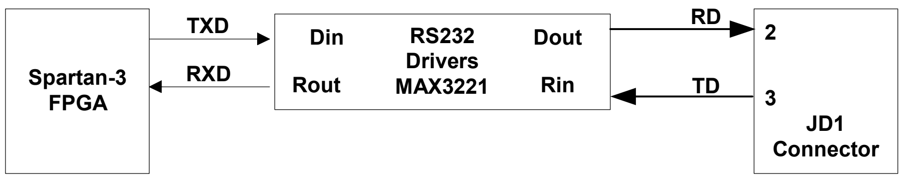

Figure 6 – RS232 Interface

Table 8 – RS232 Signal Descriptions

Signal Name	Spartan-3 Pin #	Description
RS232_RXD	A3	Data Received by FPGA
RS232_TXD	B4	Data Transmitted by FPGA

USB Port

The Spartan-3 MB development board implements a USB 2.0 port. This is accomplished using the Silicon Labs CP2101 USB-to-UART Bridge Controller. The FPGA interfaces to the CP2101 as a simple UART. The UART interface to the CP2101 can run at speeds ranging from 300 to 921,600 baud.

The CP2101 is a highly-integrated USB-to-UART Bridge Controller, providing a simple solution for USB serial communications using a minimum of components and PCB space. The CP2101 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) with full modem control signals in a compact 5mm X 5mm MLP-28 package. No other external USB components are required.

The on-chip EEPROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired. The EEPROM is programmed on-board via the USB allowing the programming step to be easily integrated into the product manufacturing and testing process.

Royalty-free Virtual COM Port (VCP) device drivers provided by Silicon Labs allow the Spartan-3 MB development board to appear as a COM port to PC applications. The CP2101 UART interface implements all RS232 signals, including control and handshaking signals. These signals are interfaced to the Spartan-3 FPGA as follows:

Table 9 – USB UART Signal Descriptions

Signal Name	Spartan-3 Pin #	Description
USB_DTR	B8	Data Terminal Ready control output (active low)
USB_RTS	A8	Ready to Send control output (active low)
USB_SOUT	B7	Asynchronous data output (UART Transmit)
USB_SIN	A6	Asynchronous data input (UART Receive)
USB_RI	B5	Ring Indicator control input (active low)
USB_DCD	B12	Data Carrier Detect control input (active low)
USB_DSR	B6	Data Set Ready control output (active low)
USB_CTS	A12	Clear To Send control input (active low)
USB_RESETn	A4	CP2101 Device Reset. Open-drain output of internal POR or VDD monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. Use FPGA pull-up to enable USB.

Driver Installation

To use the USB port, the CP2101 device drivers must be installed. These drivers are included on the Spartan-3 MB Development Kit CD, contained in the self-extracting file **CP2101.exe**. To install the CP2101 virtual COM port device drivers, do the following:

1. Double-click CP2101_Drivers.exe. The InstallShield Wizard to extract the driver installation files launches, as shown in Figure 7. Click Next.

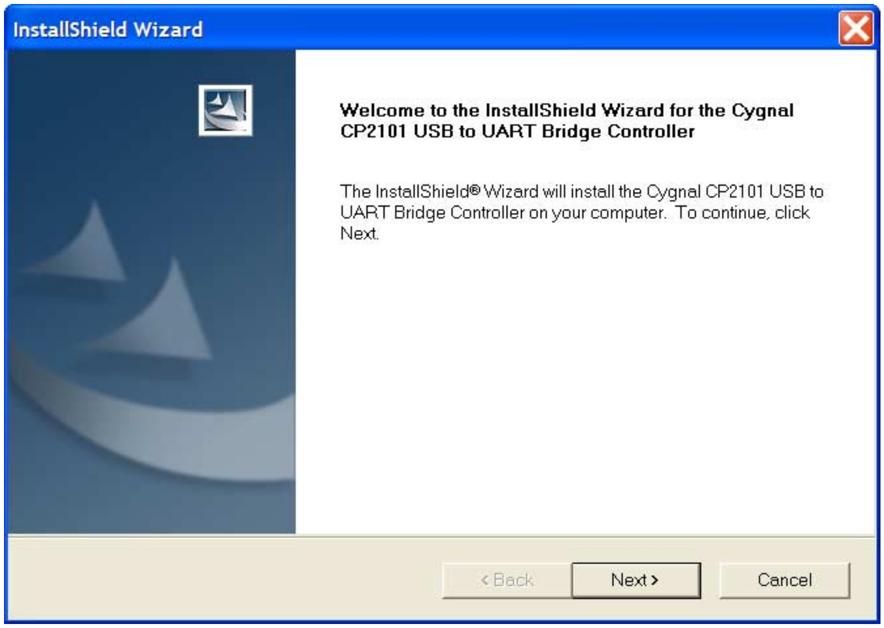

Figure 7 – Launching CP2101 Driver Installation

2. Read the license agreement and then click Yes.

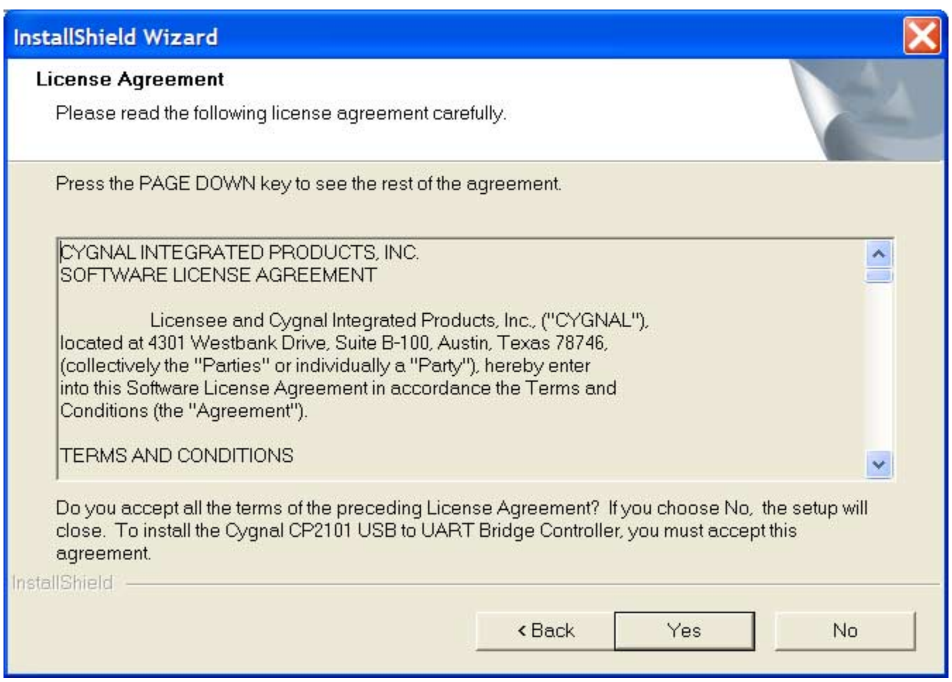

Figure 8 – Silicon Labs License Agreement

3. Browse to an acceptable installation directory, then click Next.

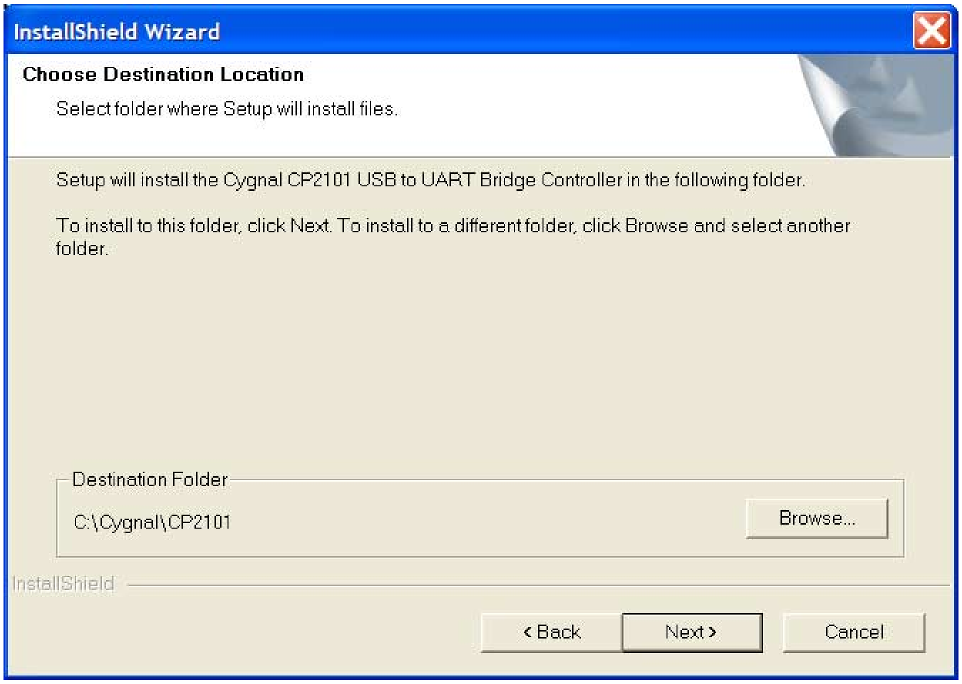

Figure 9 – CP2101 Destination Location

4. The driver installation package is extracted to the selected directory. Click Finish once the extraction completes.

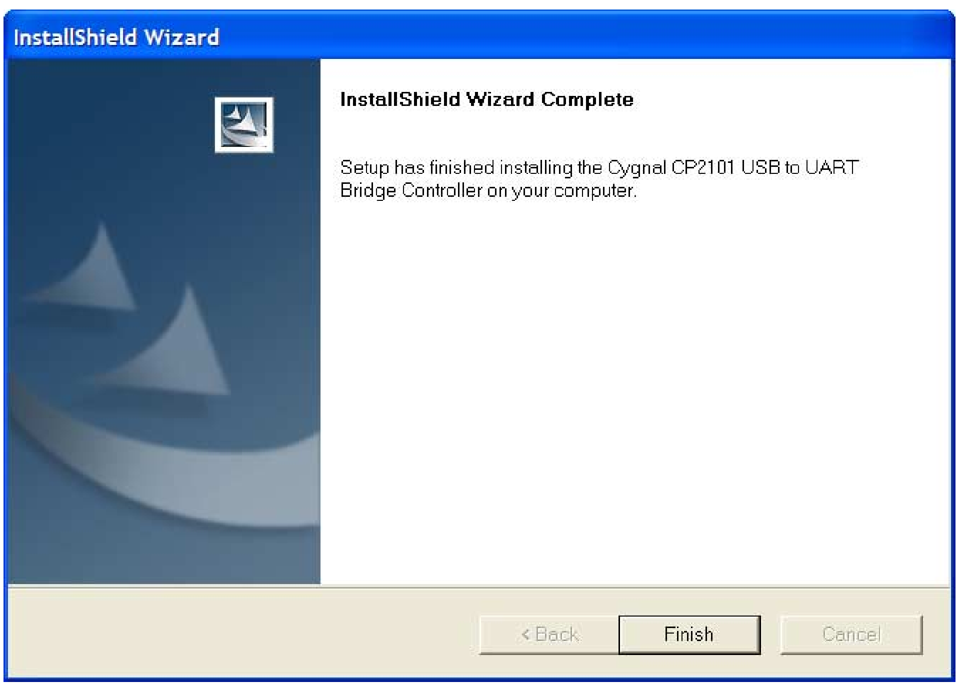

Figure 10 – CP2101 Installation Successful

5. To finish the installation, remove all J1 jumpers and install jumper JP9 in the BOARD position on a Spartan-3 MB board. Connect the 5V power supply. Turn the power switch (SW1) to ON.
6. Plug-in a USB cable from the PC to the Spartan-3 MB board. LED DS12 (USB POWER) should now be lit.
7. The **Found New Hardware Wizard** launches. Click the **Install the software automatically (Recommended)** radio button (see Figure 11) and then click Next.

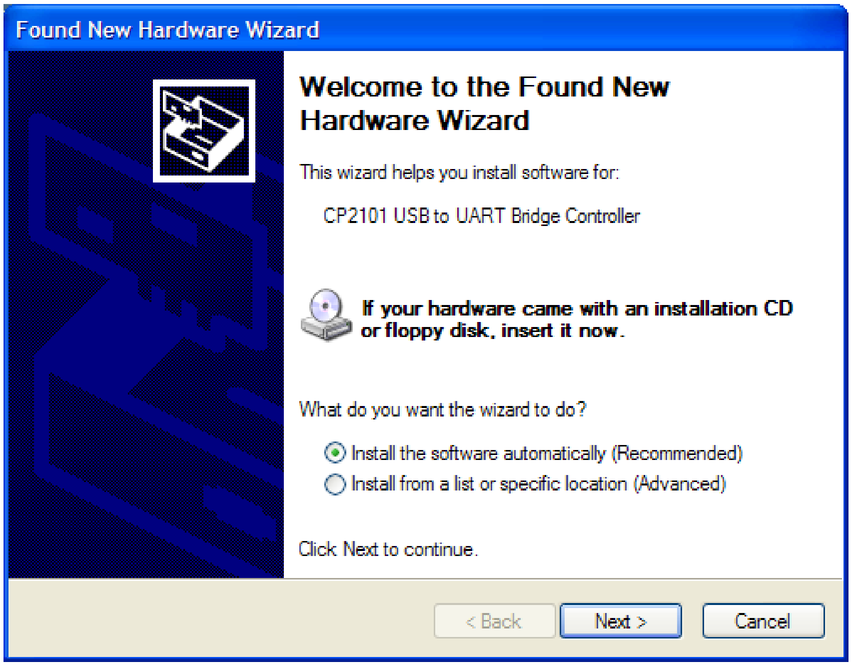

Figure 11 – Found New Hardware Wizard

8. The driver installation begins. If installing on WindowsXP, a warning is received stating that Windows Logo testing has not passed, as shown in Figure 12. Click **Continue Anyway**.

Figure 12 – Windows Logo Testing Not Passed

9. The driver installation completes at this point. Click Finish in the **Found New Hardware Wizard**.

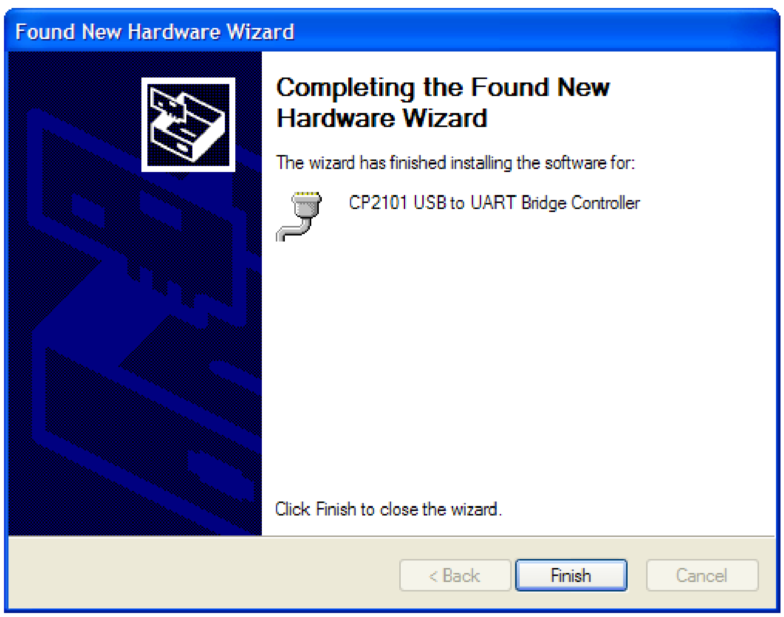

Figure 13 – CP2101 Driver Installation Complete

10. Open the Device Manager (Control Panel → System → Hardware tab → Device Manager). Under the **Ports** heading, a new device shows up, called **CP2101 USB to UART Bridge Controller**.

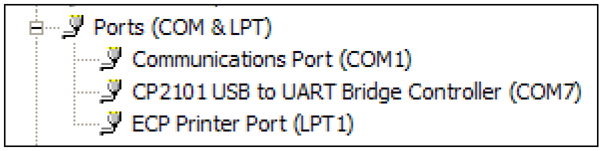

Figure 14 – CP2101 Recognized as COM Port

11. The installation is now complete. Unplug the USB cable and turn power to the OFF position.

If the installation fails, try installing the drivers manually by running C:\Silicon Labs\CP2101\WIN\Setup.exe.

Calculating the Baud Clock

Care must be taken to determine that the FPGA-created baud clock is within spec of the UART. This is important to consider, especially with the higher bauds, like 921600.

If using the Xilinx EDK opb_uartlite peripheral, the VHDL creates a RATIO based on 1/16th of the given system clock frequency and the requested baud rate. The RATIO calculation includes a truncation, which decreases the range of working system frequencies.

Based on this RATIO, the actual baud rate is created. It is recommended that the actual baud rate be within 2% of the requested baud in order for the serial communication to work.

With a 2% allowed error, the equations to use for opb_uartlite are:
RATIO = Truncate(C_CLK_FREQ / (16 * Requested_C_BAUDRATE))
Actual_C_BAUDRATE = C_CLK_FREQ / (16 * RATIO)
Error = 1 - (Requested/Actual) <= 2%

As an example, consider creating a 19200 BAUD UART from a 100 MHz system clock:
RATIO = Truncate(100M / (16 * 19200)) = 325
Actual_C_BAUDRATE = 100 M / (16 * 325) = 19230.77
Error = 1 - (19200/19230.77) = 0.16%

Since this is much less than 2%, this clock configuration works cleanly with the UART. However, consider what happens with higher bauds:

To generate 921600 from a 66.666667 MHz clock, the calculations show:
Ratio = 4
Actual_C_BAUDRATE = 1,041,667
Error = 13%

Interestingly, a 50 MHz system clock achieves:
Ratio = 3

Actual_C_BAUDRATE = 1,041,667
Error = 13%

In both of these cases, the 3SMB board USB UART will output garbled communications on the HyperTerminal.

However, if 60 MHz is the system clock, the calculations show:
Ratio = 4
Actual_C_BAUDRATE = 937,500
Error = 1.7%

75 MHz is likewise acceptable:
Ratio = 5
Actual_C_BAUDRATE = 937,500
Error = 1.7%

Both of these cases work on the 3SMB USB UART.

A spreadsheet (uartlite_clock_ratios.xls) is available on the Memec Reference Design Center that charts the calculations for the higher baud rates. The resulting values identify acceptable system clock frequencies for generating the higher baud rates.

DDR SDRAM

The Spartan-3 MB development board provides 32MB of DDR memory on the system board. This memory is implemented using the Micron MT46V16M16FG-75 16Mx16 DDR device. A high-level block diagram of the DDR interface is shown below followed by a table describing the DDR memory interface signals.

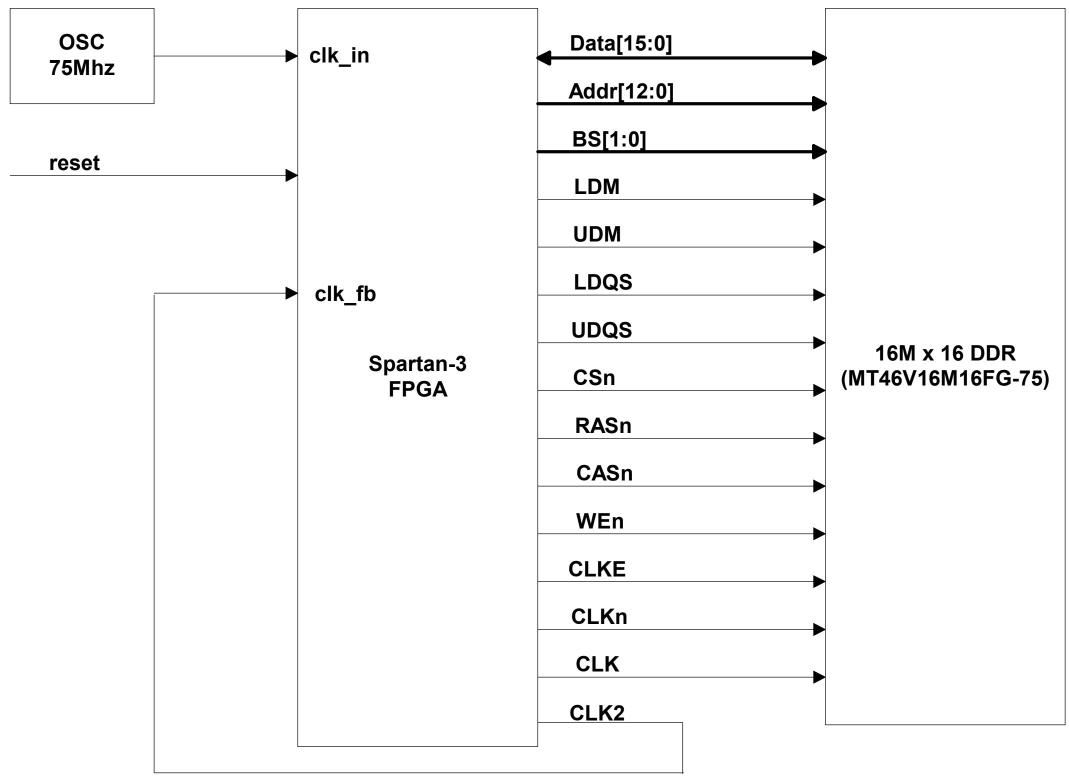

Figure 15 – DDR Interface

Table 10 – DDR Memory Interface Signal Descriptions

Signal Name	Description	FPGA Pin #	DDR Pin #
A00	Address 0	W13	K7
A01	Address 1	AE19	L8
A02	Address 2	AF15	L7
A03	Address 3	AF19	M8
A04	Address 4	AE4	M2
A05	Address 5	AB9	L3
A06	Address 6	AF4	L2
A07	Address 7	AA9	K3
A08	Address 8	AE6	K2
A09	Address 9	AC10	J3

A10	Address 10	AE15	K8
A11	Address 11	AD4	J2
A12	Address 12	AC5	H2
BA0	Bank Select 0	AD12	J8
BA1	Bank Select 1	AA10	J7
CASn	Column Address Strobe	Y11	G8
CKE	Clock Enable	AD5	H3
CLK	Positive Differential Clock to DDR	AA11	G2
CLK2	Copy of CLK	AC20	NA
clk_fb	DDR Clock input	AF14	NA
CLKn	Negative Differential Clock To DDR	AB11	G3
CSn	Chip Select	W11	H8
DM0	Low Write Mask	AB10	F7
DM1	High Write Mask	AE8	F3
DQ00	Data 0	AB13	A8
DQ01	Data 1	AB12	B9
DQ02	Data 2	AC11	B7
DQ03	Data 3	AA12	C9
DQ04	Data 4	AC13	C7
DQ05	Data 5	AA13	D9
DQ06	Data 6	AF12	D7
DQ07	Data 7	Y13	E9
DQ08	Data 8	AB7	E1
DQ09	Data 9	AC7	D3
DQ10	Data 10	AF6	D1
DQ11	Data 11	AA7	C3
DQ12	Data 12	AC6	C1
DQ13	Data 13	AE5	B3
DQ14	Data 14	AD6	B1
DQ15	Data 15	Y8	A2
DQS0	Low Write/Read Data Strobe	W12	E7
DQS1	High Write/Read Data Strobe	AA6	E3
RASn	Row Address Strobe	AB5	H7
WEn	Write Enable	AD10	G7

Flash

The Spartan-3 MB development board provides 4MB of Flash (2M x 16). One Atmel AT49BV322A-70TI is used to achieve this density. Although this is only a 16-bit data interface to the Spartan-3 device, the flash can be connected to MicroBlaze inside the Spartan-3 using an External Memory Controller (opb_emc) with data-width matching enabled (a small amount of additional glue logic required). See the Memec Reference Design Center for an example.

The following figure shows the Flash interface on the 3SMB board.

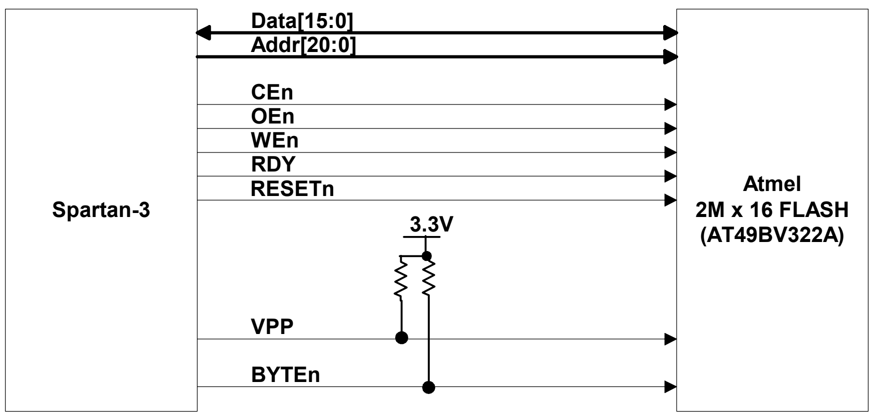

Figure 16 – Flash and SRAM Interface

Table 11 – Flash/SRAM JX Pin Assignments

Signal Name	Description	Spartan-3 Pin #	Flash Pin #
A00	Address 0	T20	25
A01	Address 1	P19	24
A02	Address 2	R19	23
A03	Address 3	R20	22
A04	Address 4	P20	21
A05	Address 5	P21	20
A06	Address 6	R21	19
A07	Address 7	P22	18
A08	Address 8	U23	8
A09	Address 9	P26	7
A10	Address 10	P25	6
A11	Address 11	R26	5
A12	Address 12	R25	4
A13	Address 13	T26	3
A14	Address 14	T25	2
A15	Address 15	U26	1

A16	Address 16	U25	48
A17	Address 17	R22	17
A18	Address 18	T22	16
A19	Address 19	U24	9
A20	Address 20	T23	10
BYTEn	Word/Byte select	U20	47
CEn	Chip enable	V25	26
D00	Data 0	V21	29
D01	Data 1	T21	31
D02	Data 2	V22	33
D03	Data 3	AB23	35
D04	Data 4	W23	38
D05	Data 5	V23	40
D06	Data 6	Y25	42
D07	Data 7	W25	44
D08	Data 8	U21	30
D09	Data 9	W22	32
D10	Data 10	U22	34
D11	Data 11	AB24	36
D12	Data 12	W24	39
D13	Data 13	V24	41
D14	Data 14	Y26	43
D15	Data 15/Address -1 (LSB for byte transactions)	W26	45
OEn	Output Enable	T19	28
RDY	Ready/Busy_n	P24	15
RESETn	Reset	P23	12
VPP	Write protection	V20	14
WEn	Write enable	R24	11

LVDS

The Spartan-3 MB development board provides a complete high-performance differential signaling (LVDS) interface, enabling the designers to prototype high-speed serial communication links. The Spartan-3 I/Os are designed to comply with the IEEE electrical specifications for LVDS to make system and board design easier. With the addition of an LVDS current-mode driver in the IOBs, which eliminates the need for external source termination in point-to-point applications, and with the choice of two different voltage modes and an extended mode, Spartan-3 devices provide a flexible solution for doing an LVDS design in an FPGA.

LVDS Interface

The Spartan-3 MB development board provides an 8-bit LVDS port (Transmit and Receive) with two additional control signals. The following figure shows the LVDS interface on the Spartan-3 MB development board. LVDS termination networks are provided between the Spartan-3 FPGA and the LVDS user connectors. It should be noted that no LVDS source terminations are needed when using the Spartan-3 FPGA family in point-to-point applications.

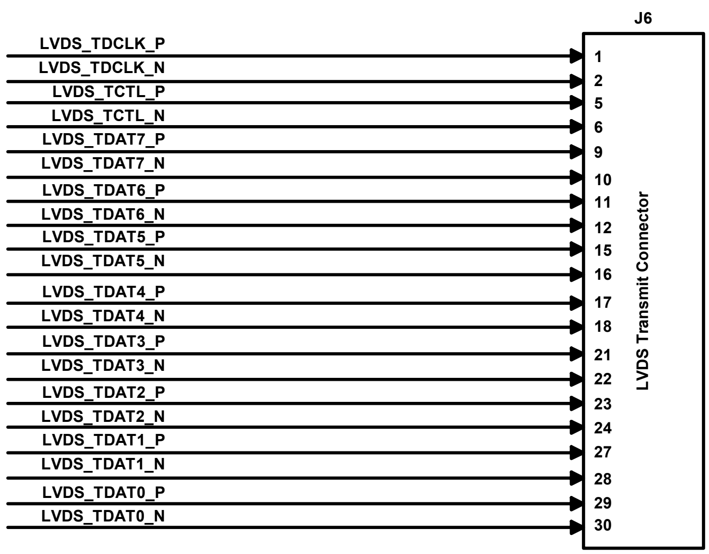

Figure 17 – LVDS Transmit Port

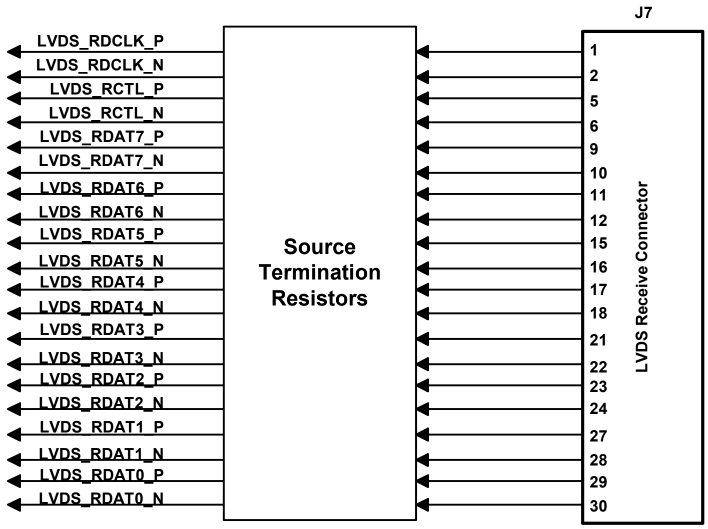

Figure 18 – LVDS Receive Port

LVDS Port Signal Descriptions

The following table shows the LVDS port signal descriptions and the port signal assignments to the Spartan-3 FPGA.

Table 12 – LVDS Transmit Port Signal Descriptions

Signal Name	Description	Spartan-3 Pin #	J6 Pin #
LVDS_TDCLK_P	Positive Transmit Clock	B15	1
LVDS_TDCLK_N	Negative Transmit Clock	A15	2
GND	Ground	NA	3
GND	Ground	NA	4
LVDS_TCTL_P	Positive Transmit Control	B19	5
LVDS_TCTL_N	Negative Transmit Control	A19	6
GND	Ground	NA	7
GND	Ground	NA	8
LVDS_TDAT7_P	Positive Data Transmit Bit 7	B20	9
LVDS_TDAT7_N	Negative Data Transmit Bit 7	A20	10
LVDS_TDAT6_P	Positive Data Transmit Bit 6	B21	11
LVDS_TDAT6_N	Negative Data Transmit Bit 6	A21	12
GND	Ground	NA	13
GND	Ground	NA	14
LVDS_TDAT5_P	Positive Data Transmit Bit 5	E17	15
LVDS_TDAT5_N	Negative Data Transmit Bit 5	D17	16
LVDS_TDAT4_P	Positive Data Transmit Bit 4	E20	17
LVDS_TDAT4_N	Negative Data Transmit Bit 4	D20	18
GND	Ground	NA	19
GND	Ground	NA	20
LVDS_TDAT3_P	Positive Data Transmit Bit 3	D21	21
LVDS_TDAT3_N	Negative Data Transmit Bit 3	C21	22
LVDS_TDAT2_P	Positive Data Transmit Bit 2	C22	23

LVDS_TDAT2_N	Negative Data Transmit Bit 2	B22	24
GND	Ground	NA	25
GND	Ground	NA	26
LVDS_TDAT1_P	Positive Data Transmit Bit 1	C23	27
LVDS_TDAT1_N	Negative Data Transmit Bit 1	B23	28
LVDS_TDAT0_P	Positive Data Transmit Bit 0	C26	29
LVDS_TDAT0_N	Negative Data Transmit Bit 0	C25	30

Table 13 – LVDS Receive Port Signal Descriptions

Signal Name	Description	Spartan-3 Pin #	J6 Pin #
LVDS_RDCLK_P	Positive Receive Clock	C14	1
LVDS_RDCLK_N	Negative Receive Clock	B14	2
GND	Ground	NA	3
GND	Ground	NA	4
LVDS_RCTL_P	Positive Receive Control	E24	5
LVDS_RCTL_N	Negative Receive Control	E23	6
GND	Ground	NA	7
GND	Ground	NA	8
LVDS_RDAT7_P	Positive Data Receive Bit 7	D26	9
LVDS_RDAT7_N	Negative Data Receive Bit 7	D25	10
LVDS_RDAT6_P	Positive Data Receive Bit 6	H24	11
LVDS_RDAT6_N	Negative Data Receive Bit 6	H23	12
GND	Ground	NA	13
GND	Ground	NA	14
LVDS_RDAT5_P	Positive Data Receive Bit 5	H26	15
LVDS_RDAT5_N	Negative Data Receive Bit 5	H25	16
LVDS_RDAT4_P	Positive Data Receive Bit 4	K24	17
LVDS_RDAT4_N	Negative Data Receive Bit 4	K23	18
GND	Ground	NA	19
GND	Ground	NA	20
LVDS_RDAT3_P	Positive Data Receive Bit 3	K26	21
LVDS_RDAT3_N	Negative Data Receive Bit 3	K25	22
LVDS_RDAT2_P	Positive Data Receive Bit 2	M26	23
LVDS_RDAT2_N	Negative Data Receive Bit 2	M25	24
GND	Ground	NA	25
GND	Ground	NA	26
LVDS_RDAT1_P	Positive Data Receive Bit 1	N24	27
LVDS_RDAT1_N	Negative Data Receive Bit 1	N23	28
LVDS_RDAT0_P	Positive Data Receive Bit 0	N26	29
LVDS_RDAT0_N	Negative Data Receive Bit 0	N25	30

Piezo Speaker

The Spartan-3 MB development board provides a piezo speaker output for generating simple tones. The Piezo is connected to the Spartan-3 FPGA via pin AC26.

10/100 Ethernet

The Spartan-3 MB development board provides a 10/100 Ethernet PHY interface. The Broadcom BCM5221 implements the PHY function while the 10/100 Ethernet MAC must reside inside the FPGA device. The following figure shows a high-level block diagram of the 10/100 interface on the 3SMB board.

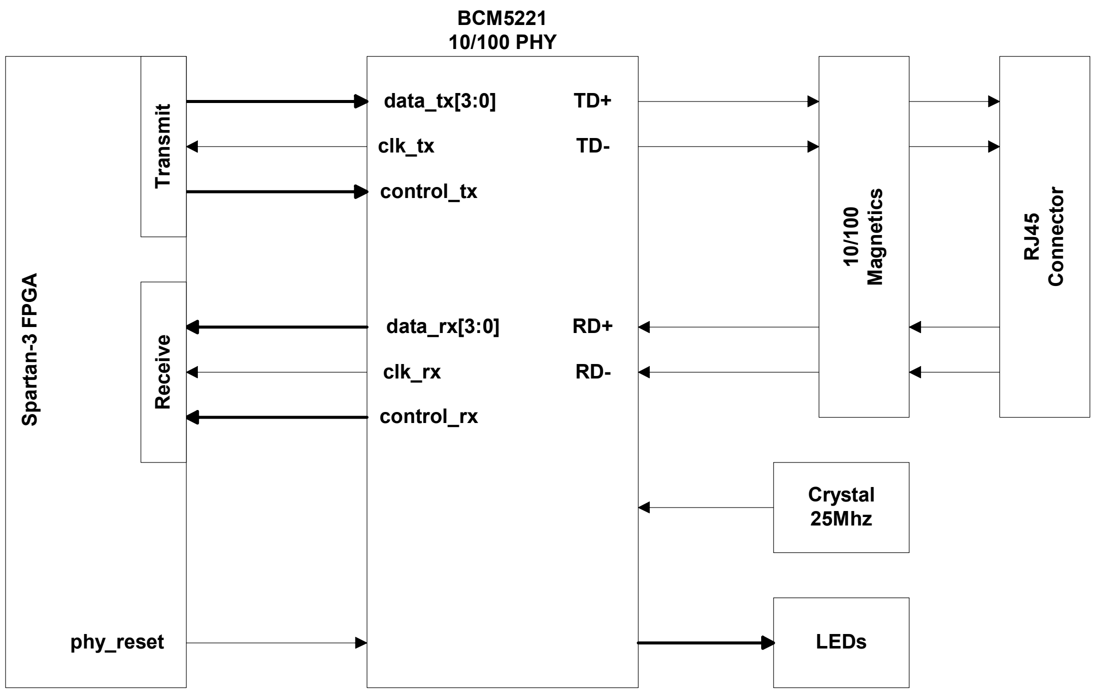

Figure 19 – 10/100 Ethernet Interface

Table 14 – Ethernet Pin Assignments

Signal Name	Spartan-3 Pin #
ETH_COL	AF22
ETH_CRS	AE21
ETH_MDC	AD23
ETH_MDIO	AD21
ETH_RXC	W16
ETH_RXD0	Y16
ETH_RXD1	AA17
ETH_RXD2	AA18
ETH_RXD3	AA20
ETH_RXDV	Y18
ETH_RXER	W15
ETH_TXC	AC21
ETH_TXD0	AF24
ETH_TXD1	AE23
ETH_TXD2	AF23
ETH_TXD3	AE22
ETH_TXEN	AE24
ETH_TXER	AB21
PHY_RESETn	AF21

Configuration Support

The Spartan-3 MB development board supports three different FPGA configuration methods, which are described below.

JTAG Port

A 2x7 Parallel-IV JTAG connector provides an interface to the board's JTAG chain, as shown in Figure 20. This chain can be used to program the on-board ISP PROM and configure the Spartan-3 FPGA. The Spartan-3 MB board's JTAG chain consists of an XCF04S Platform Flash PROM followed by an XCF01S followed by an XC3S1500 FPGA using a 3.3V interface (series protection resistors required for Spartan-3).

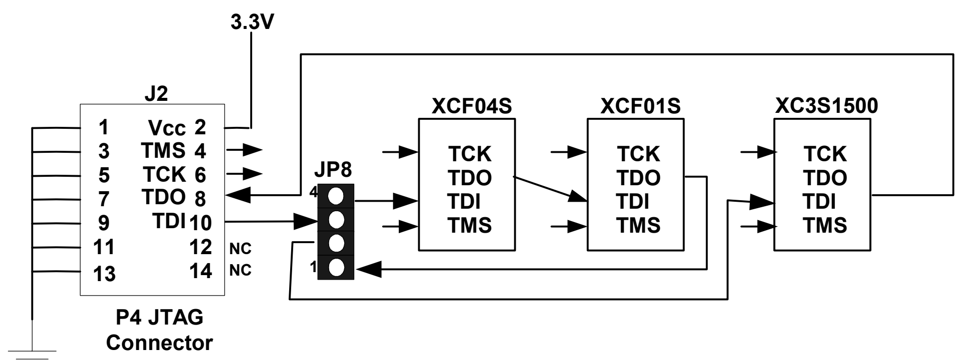

Figure 20 – JTAG Chain Description

The Xilinx Parallel-IV cable is the recommended solution for configuring the 3SMB JTAG chain. Using Parallel-III is possible, but the user must use a P4-to-P3 adapter or plug into the connections on JP11.

Platform Flash ISP PROM

The Spartan-3 MB development board utilizes the Xilinx Platform Flash In-System Programmable (ISP) PROMs, allowing designers to store an FPGA design in non-volatile memory. The XC3S1500 device requires approximately 5Mbit for configuration. Therefore, 4Mbit (XCF04S) and 1Mbit (XCF01S) PROMs are cascaded together to contain the FPGA bitstream.

The JTAG port on the Platform Flash device is used to program the PROM with an .mcs file created by iMPACT in the Xilinx ISE software environment. The PROM can be programmed with the .mcs file through the JTAG port or using an external programmer like the Xilinx MultiPRO.

Once the Platform Flash has been programmed, the user can configure the Spartan-3 device by setting the Configuration Mode to Master Serial Mode (see Table 15). The Spartan-3 device configuration is initiated during power-up or by asserting the PROGAMn signal (by pressing the SW2 switch). Upon activation of the PROGAMn signal, the Platform Flash devices will use their FPGA Configuration Port to configure the Spartan-3 FPGA.

If the Spartan-3 configuration mode (J1) is set to Master Serial, the PROM's D0, CE, CCLK, RESET/OE, and the CF signals are used to configure the FPGA.

Controlling CCLK

The configuration clock, CCLK, provides the clock to the PROMs so that data can be read. In Master Serial Mode, the FPGA generates and outputs CCLK to the PROMs. In some cases, it is desirable to put additional information in any leftover space in the PROMs, such as a unique serial number or MAC address.

On the 3SMB board, an additional I/O pin is connected to the CCLK net. This allows the user to provide additional pulses on the CCLK input to the PROMs to retrieve additional data after configuration is over. This I/O is Spartan-3 Pin number AB20.

Program Switch (SW2)

The Spartan-3 MB development board provides a push button switch for initiating Spartan-3 FPGA configuration. After programming both Platform Flash devices, this switch asserts the PROGAMn signal. Upon assertion of the PROGAMn signal, the Spartan-3 FPGA clears its configuration memory and then initiates reconfiguration from the Platform Flash.

Mode Select

The Spartan-3 FPGA Mode pins determine how the FPGA will respond when the FPGA initiates a configuration sequence, either during power-up or when the PROGRAM button is pushed. Table 15 shows the Spartan-3 Configuration Mode Select jumper settings. This table is also printed on the solder side of the Spartan-3 MB PCB.

Table 15 – Spartan-3 Configuration Mode Select

Mode	J1		
	5-6 (M2)	3-4 (M1)	1-2 (M0)
Master Serial	Closed	Closed	Closed
Slave Serial	Open	Open	Open
Master Parallel	Closed	Open	Open
Slave Parallel	Open	Open	Closed
JTAG	Open	Closed	Open

When Mode Jumper M3 is installed, configuration pull-ups are implemented.

SystemACE Connector

The Spartan-3 MB development board provides a SystemACE interface that can be used to configure the Spartan-3 FPGA. The interface also gives software designers the ability to create a file system on the removable CompactFlash card. The Memec Design

SystemACE module (DS-KIT-SYSTEMACE – sold separately) can be used to perform both of these functions.

The SystemACE connector can also be used for general purpose I/O when not using the SystemACE module.

The following figure shows a high-level block diagram of the Memec SystemACE module. For more information, please refer to the Memec SystemACE Module User's Guide.

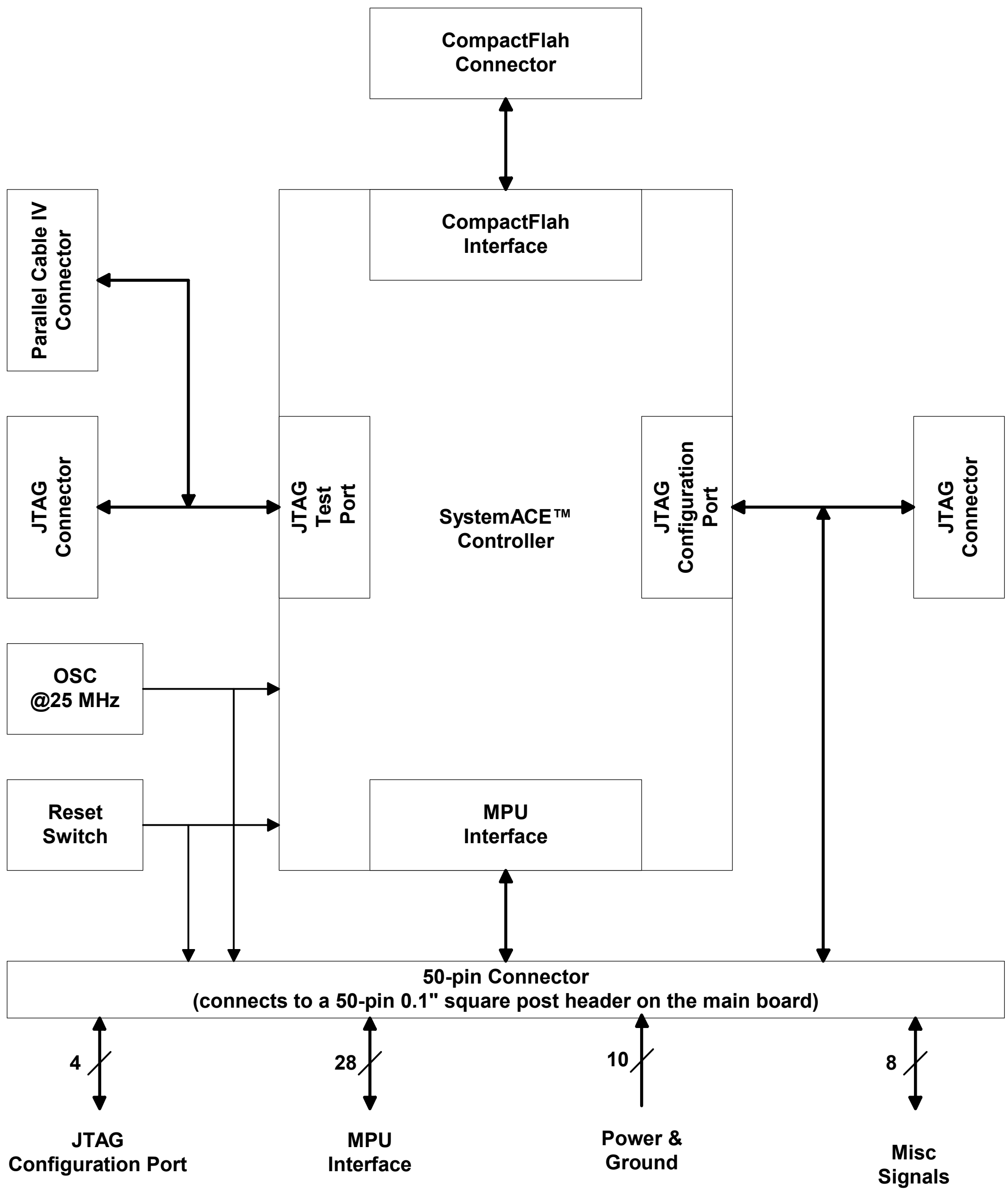

Figure 21 – SystemACE Module Block Diagram

When the MPU port of the SystemACE controller is used, the FPGA and the SystemACE controller must use the same clock source. Hence, a jumper is provided on the Spartan-3 MB development board and the SystemACE module to provide the clock input to both devices. The following table shows the required jumper connections.

Table 16 – SystemACE Controller Clock Source

Clock Source	Jumper Settings	
	JP10 (3SMB board)	JP5 (SAM board)
SystemACE module 25Mhz OSC	Jumper 1-3	Open (25MHz osc enabled)
FPGA-generated clock < 33 MHz output on P10	Jumper 1-2, 3-4	Close

The following table shows the SystemACE interface signals. A 50-pin 0.1" square post header (JP11) is used to connect the SystemACE module to the 3SMB development board.

The pin-out for Spartan-3 I/O on JP11 is shown in Table 17

Table 17 – SystemACE Connector Signal Description

Spartan-3 Pin #	SystemACE Signal Name	JP29 Pin #		SystemACE Signal Name	Spartan-3 Pin #
	3.3V	1	2	**3.3V**	
	TDO	3	4	**GND**	
	TMS	5	6	CLOCK	
	TDI	7	8	**GND**	
	PROGRAMn	9	10	TCK	
	GND	11	12	**GND**	
F14	OEn	13	14	INITn	
D14	MPA0	15	16	WEn	E14
E15	MPA2	17	18	MPA1	C15
	2.5V	19	20	MPA3	D16
C17	MPD00	21	22	**2.5V**	
E18	MPD02	23	24	MPD01	F17
F20	MPD04	25	26	MPD03	G19
D22	MPD06	27	28	MPD05	E21
H14	MPD08	29	30	MPD07	E22
G14	MPD10	31	32	MPD09	G15
F16	MPD12	33	34	MPD11	F15
G17	MPD14	35	36	MPD13	E16
G18	MPA4	37	38	MPD15	F18
A14	MPA6	39	40	MPA5	F21
H15	IRQ	41	42	**GND**	
G16	RESETn	43	44	CEn	H16
	DONE	45	46	BRDY	A22
	CCLK	47	48	BITSTREAM	
	GND	49	50	**NC**	

P160 Expansion Slots

Two P160 expansion slots are included on the Spartan-3 MB development board to support plug-in modules for various applications. The following tables show the Spartan-3 pin assignments to the P160 expansion slot connectors (JX1 & JX2 for Slot A, JX3 & JX4 for Slot B) located on the Spartan-3 MB development board.

Table 18 – Slot A Left Header (JX1) Signal Assignments

FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	FPGA Pin #
	TCK	A1	B1	FPGA.BITSTREAM	
	GND	A2	B2	SM.DOUT/BUSY	
	TMS	A3	B3	FPGA.CCLK	
	Vin	A4	B4	DONE	
	TDI	A5	B5	INITn	
	GND	A6	B6	PROGRAMn	
	TDO	A7	B7	NC	
	3.3V	A8	B8	LIOB8	H5
M5	LIOA9	A9	B9	LIOB9	J5
	GND	A10	B10	LIOB10	K5
M3	LIOA11	A11	B11	LIOB11	L5
	2.5V	A12	B12	LIOB12	M6
N8	LIOA13	A13	B13	LIOB13	N6
	GND	A14	B14	LIOB14	N7
W4	LIOA15	A15	B15	LIOB15	AD13
	Vin	A16	B16	LIOB16	J6
N4	LIOA17	A17	B17	LIOB17	K6
	GND	A18	B18	LIOB18	L6
N3	LIOA19	A19	B19	LIOB19	M7
	3.3V	A20	B20	LIOB20	M8
N5	LIOA21	A21	B21	LIOB21	E3
	GND	A22	B22	LIOB22	J7
P3	LIOA23	A23	B23	LIOB23	K7
	2.5V	A24	B24	LIOB24	L7
P4	LIOA25	A25	B25	LIOB25	L8
	GND	A26	B26	LIOB26	P1
R3	LIOA27	A27	B27	LIOB27	P2
	Vin	A28	B28	LIOB28	R1
T4	LIOA29	A29	B29	LIOB29	R2
	GND	A30	B30	LIOB30	T1
U4	LIOA31	A31	B31	LIOB31	T2
	3.3V	A32	B32	LIOB32	U1
U3	LIOA33	A33	B33	LIOB33	U2
	GND	A34	B34	LIOB34	V2
V4	LIOA35	A35	B35	LIOB35	W1
	2.5V	A36	B36	LIOB36	W2
V3	LIOA37	A37	B37	LIOB37	AC1
	GND	A38	B38	LIOB38	AC2
AE13	LIOA39	A39	B39	LIOB39	AD1
	Vin	A40	B40	LIOB40	AD2

Table 19 – Slot A Right Header (JX2) Signal Assignments

FPGA Pin #	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	FPGA Pin #
K3	RIOA1	A1	B1	**GND**	
K4	RIOA2	A2	B2	RIOB2	L4
J3	RIOA3	A3	B3	**Vin**	
J4	RIOA4	A4	B4	RIOB4	N1
H3	RIOA5	A5	B5	**GND**	
H4	RIOA6	A6	B6	RIOB6	B3
N2	RIOA7	A7	B7	**3.3V**	
M1	RIOA8	A8	B8	RIOB8	C4
M2	RIOA9	A9	B9	**GND**	
L1	RIOA10	A10	B10	RIOB10	E5
L2	RIOA11	A11	B11	**2.5V**	
K1	RIOA12	A12	B12	RIOB12	C5
K2	RIOA13	A13	B13	**GND**	
J2	RIOA14	A14	B14	RIOB14	D5
H1	RIOA15	A15	B15	**Vin**	
H2	RIOA16	A16	B16	RIOB16	C6
G1	RIOA17	A17	B17	**GND**	
G2	RIOA18	A18	B18	RIOB18	D6
D1	RIOA19	A19	B19	**3.3V**	
D2	RIOA20	A20	B20	RIOB20	D7
F6	RIOA21	A21	B21	**GND**	
E7	RIOA22	A22	B22	RIOB22	F9
A7	RIOA23	A23	B23	**2.5V**	
H11	RIOA24	A24	B24	RIOB24	D10
F10	RIOA25	A25	B25	**GND**	
G10	RIOA26	A26	B26	RIOB26	C10
G11	RIOA27	A27	B27	**Vin**	
H12	RIOA28	A28	B28	RIOB28	D11
H13	RIOA29	A29	B29	**GND**	
E4	RIOA30	A30	B30	RIOB30	E11
F5	RIOA31	A31	B31	**3.3V**	
E6	RIOA32	A32	B32	RIOB32	C12
F7	RIOA33	A33	B33	**GND**	
G9	RIOA34	A34	B34	RIOB34	E12
E10	RIOA35	A35	B35	**2.5V**	
F11	RIOA36	A36	B36	RIOB36	C13
F12	RIOA37	A37	B37	**GND**	
G12	RIOA38	A38	B38	RIOB38	D13
F13	RIOA39	A39	B39	**Vin**	
G13	RIOA40	A40	B40	RIOB40	E13

Table 20 – Slot B Left Header (JX3) Signal Assignments

FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	FPGA Pin #
	TCK	A1	B1	FPGA.BITSTREAM	
	GND	A2	B2	SM.DOUT/BUSY	
	TMS	A3	B3	FPGA.CCLK	
	Vin	A4	B4	DONE	
	TDI	A5	B5	INITn	
	GND	A6	B6	PROGRAMn	
	TDO	A7	B7	NC	
	3.3V	A8	B8	LIOB8	K20
G8	LIOA9	A9	B9	LIOB9	J22
	GND	A10	B10	LIOB10	J23
G5	LIOA11	A11	B11	LIOB11	J20
	2.5V	A12	B12	LIOB12	A23
B13	LIOA13	A13	B13	LIOB13	F19
	GND	A14	B14	LIOB14	E19
AE16	LIOA15	A15	B15	LIOB15	D19
	Vin	A16	B16	LIOB16	C19
AF17	LIOA17	A17	B17	LIOB17	C18
	GND	A18	B18	LIOB18	B18
AE17	LIOA19	A19	B19	LIOB19	D18
	3.3V	A20	B20	LIOB20	A17
AE18	LIOA21	A21	B21	LIOB21	B17
	GND	A22	B22	LIOB22	A16
AD18	LIOA23	A23	B23	LIOB23	B16
	2.5V	A24	B24	LIOB24	E9
F1	LIOA25	A25	B25	LIOB25	E8
	GND	A26	B26	LIOB26	F8
G7	LIOA27	A27	B27	LIOB27	B11
	Vin	A28	B28	LIOB28	A11
E2	LIOA29	A29	B29	LIOB29	B10
	GND	A30	B30	LIOB30	A10
E1	LIOA31	A31	B31	LIOB31	D9
	3.3V	A32	B32	LIOB32	B9
AC18	LIOA33	A33	B33	LIOB33	C9
	GND	A34	B34	LIOB34	C8
AB18	LIOA35	A35	B35	LIOB35	D8
	2.5V	A36	B36	LIOB36	F4
F2	LIOA37	A37	B37	LIOB37	F3
	GND	A38	B38	LIOB38	G4
H7	LIOA39	A39	B39	LIOB39	G6
	Vin	A40	B40	LIOB40	H6

Table 21 – Slot B Right Header (JX4) Signal Assignments

FPGA Pin #	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	FPGA Pin #
AB26	RIOA1	A1	B1	**GND**	
AB25	RIOA2	A2	B2	RIOB2	AA25
AA26	RIOA3	A3	B3	**Vin**	
E25	RIOA4	A4	B4	RIOB4	G20
E26	RIOA5	A5	B5	**GND**	
F25	RIOA6	A6	B6	RIOB6	H20
F26	RIOA7	A7	B7	**3.3V**	
G25	RIOA8	A8	B8	RIOB8	L20
G26	RIOA9	A9	B9	**GND**	
F24	RIOA10	A10	B10	RIOB10	L19
F23	RIOA11	A11	B11	**2.5V**	
G23	RIOA12	A12	B12	RIOB12	G21
H22	RIOA13	A13	B13	**GND**	
J24	RIOA14	A14	B14	RIOB14	G22
K22	RIOA15	A15	B15	**Vin**	
L22	RIOA16	A16	B16	RIOB16	H21
L23	RIOA17	A17	B17	**GND**	
M24	RIOA18	A18	B18	RIOB18	J21
M22	RIOA19	A19	B19	**3.3V**	
N22	RIOA20	A20	B20	RIOB20	J25
N21	RIOA21	A21	B21	**GND**	
N20	RIOA22	A22	B22	RIOB22	K21
N19	RIOA23	A23	B23	**2.5V**	
W21	RIOA24	A24	B24	RIOB24	L21
Y22	RIOA25	A25	B25	**GND**	
Y23	RIOA26	A26	B26	RIOB26	L26
AA24	RIOA27	A27	B27	**Vin**	
AA23	RIOA28	A28	B28	RIOB28	L25
Y7	RIOA29	A29	B29	**GND**	
Y6	RIOA30	A30	B30	RIOB30	M21
Y5	RIOA31	A31	B31	**3.3V**	
Y4	RIOA32	A32	B32	RIOB32	M20
AA4	RIOA33	A33	B33	**GND**	
AA3	RIOA34	A34	B34	RIOB34	M19
Y2	RIOA35	A35	B35	**2.5V**	
AB2	RIOA36	A36	B36	RIOB36	W20
AA2	RIOA37	A37	B37	**GND**	
AB1	RIOA38	A38	B38	RIOB38	Y20
AA1	RIOA39	A39	B39	**Vin**	
Y1	RIOA40	A40	B40	RIOB40	Y21

Power System Design

The Spartan-3 MB development board's power system is designed to meet the required Xilinx power specifications for the Spartan-3 FPGA on all three rails: V_{CCINT}, V_{CCAUX}, and V_{CCO}. These specifications include:

- $V_{NOMINAL}$ +/- 5%
- Monotonic ramp on V_{CCINT}, V_{CCAUX}, and $V_{CCO-Bank4}$
- V_{CCO} Ramp Time > 0.6ms

Although not required, V_{CCINT} and V_{CCAUX} were designed to allow an adjustable ramp time. This is helpful in controlling the power-on surge current from the bypass capacitors, which in turn helps to achieve a monotonic rise.

The Spartan-3 MB development board incorporates a 5V supervisor and staggered power-up to reduce the instantaneous demand on the input power supply. Note that this sequencing is NOT required by the Spartan-3 FPGA (see the Spartan-3 datasheet for more details).

Three sources are available for the 5V input supply. The primary source is a 5V/3A AC/DC converter included in the Spartan-3 MB Development Kit.

Secondly, the USB port is capable of providing 5V/500mA. To power the board from the USB port, do the following:

- Install JP2
- Move the jumper on JP9 to the "JACK" position
- Slide SW1 to the OFF position
- Plug in a USB cable from a PC to the board

A user-supplied 5V source can also be easily connected to the board through the 5V pad near SW2.

As shown in the schematic, 5V is regulated to 1.2V, 2.5V, and 3.3V. The 2.5V and 3.3V circuits use the Texas Instruments' TPS40003 switching controller for efficient regulation at 3A each. The TPS40K series was specifically chosen because the soft-start is user-controllable by changing the circuit components. Since both 2.5V and 3.3V are used to power VCCo on the eight I/O banks, both had a requirement to ramp slower than 0.6 ms.

The TPS64203 is used to regulate 3A at 1.2V. This circuit is simpler than the TPS40K designs, but the soft-start is not user-controllable.

The TI TPS3806 is a dual-voltage supervisor. For the 3SMB, it monitors 5V on the primary channel, enabling the 2.5V TPS40K circuit. On the secondary channel, the TPS3806 monitors 2.5V, which in turn enables the 3.3V TPS40K circuit.

The TI TLC7725 supervisor monitors 3.3V and enables the 1.2V TPS64203 circuit.

The regulators can be disabled by installing jumpers on JP12 (1.2V disable), JP5 (2.5V disable), or JP13 (3.3V disable).

Besides VIN (5V), voltage input pads are included on the board for 3.3V, 2.5V, and 1.2V if user-supplied power is preferred.

Littelfuse resettable fuses are included in the power system design for 3.3V, 2.5V, and 1.2V. This protects the board from any unforeseen current surges. It also gives the user an ideal point of contact on the board to add a current loop for measuring the current draw on each of the three rails.

Revision History

Date	Version	Revision
09/27/04	2.0	Initial Memec release.
01/13/05	2.1	Fixed the block diagram in Figure 3
06/02/05	2.2	Fixed typos in USB installation instructions

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