3SMB

REV2

BOARD NAME :	**SPARTAN 3 MB BOARD**
BOARD PART NUMBER :	**DS-BD-3SxxxxMB-FG676**
BOARD REVISION :	**2**

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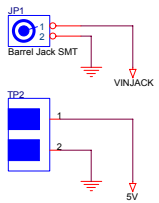
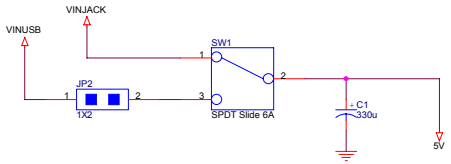
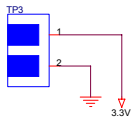
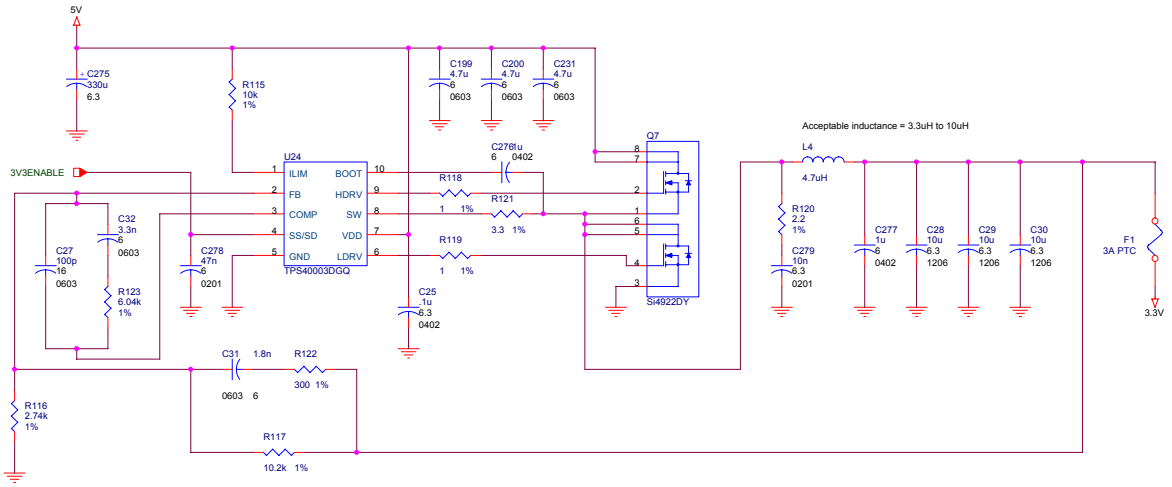
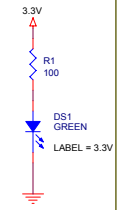
VOLTAGE	INPUT JACK	REGULATION	LED	SUPERVISOR
VIN (5V)				
3.3V				
2.5V				

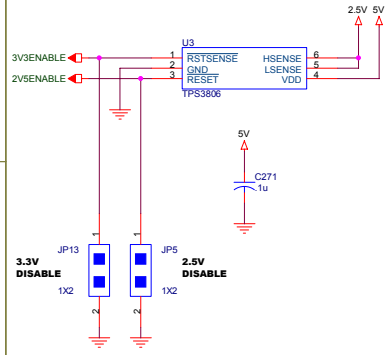


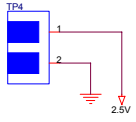


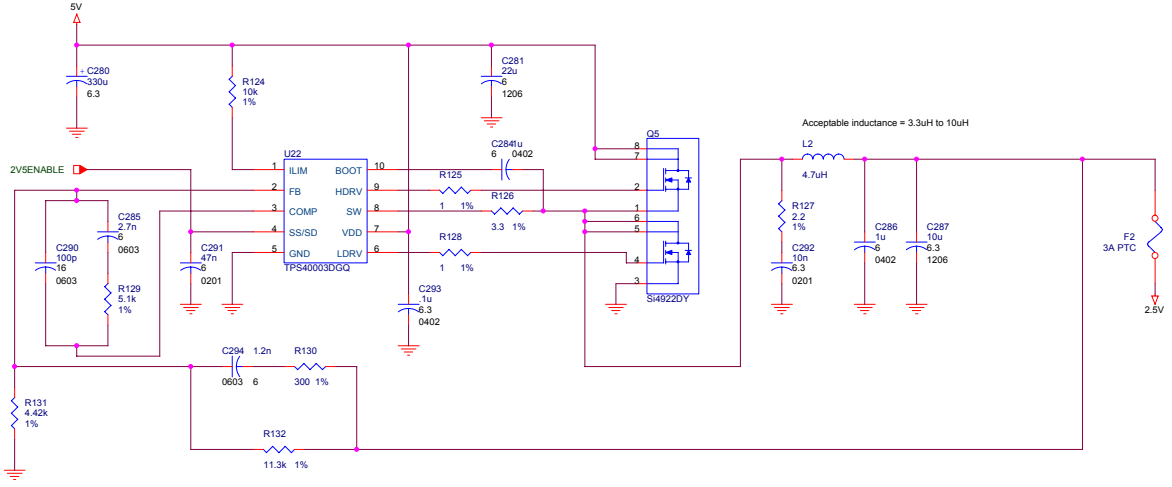


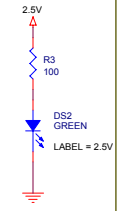












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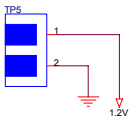
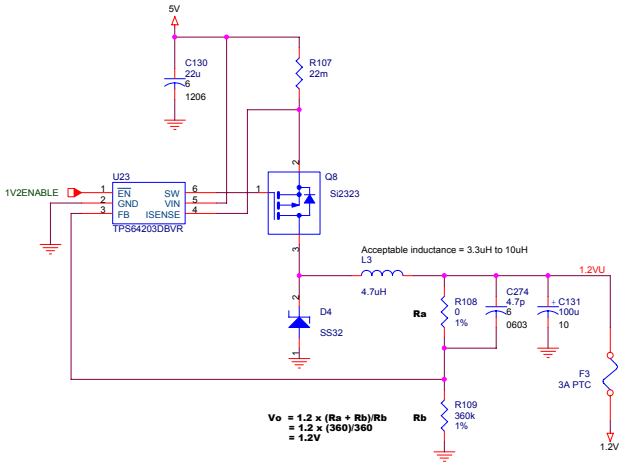
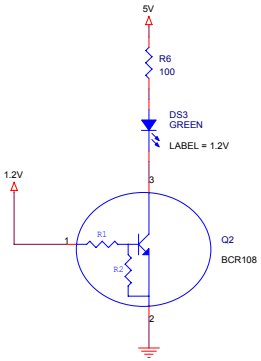
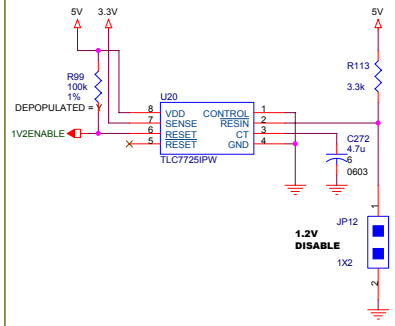
1.2V









GROUND TEST LOOPS

FEET

NE1 Little Rubber Feet -Thick
MOUNT TO BOTTOM AS PER SSB
NE3 Little Rubber Feet -Thick
MOUNT TO BOTTOM AS PER SSB
NE4 Little Rubber Feet -Thick
MOUNT TO BOTTOM AS PER SSB
NE5 Little Rubber Feet -Thick
MOUNT TO BOTTOM AS PER SSB
NE26 Little Rubber Feet -Thick
MOUNT TO BOTTOM AS PER SSB
NE27 Little Rubber Feet -Thick
MOUNT TO BOTTOM AS PER SSB

MOUNTING HOLES

NE6 Mounting Hole (.125)
NE7 Mounting Hole (.125)
NE8 Mounting Hole (.125)
NE10 Mounting Hole (.125)

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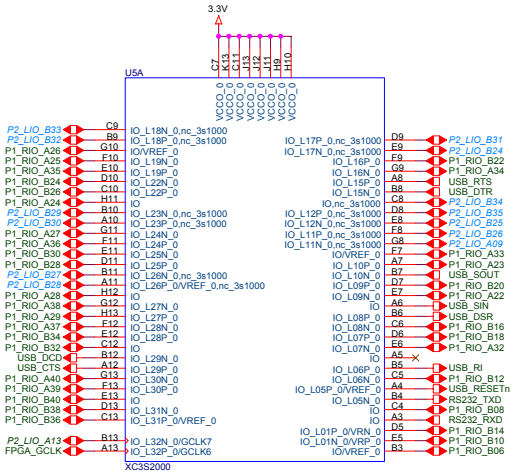
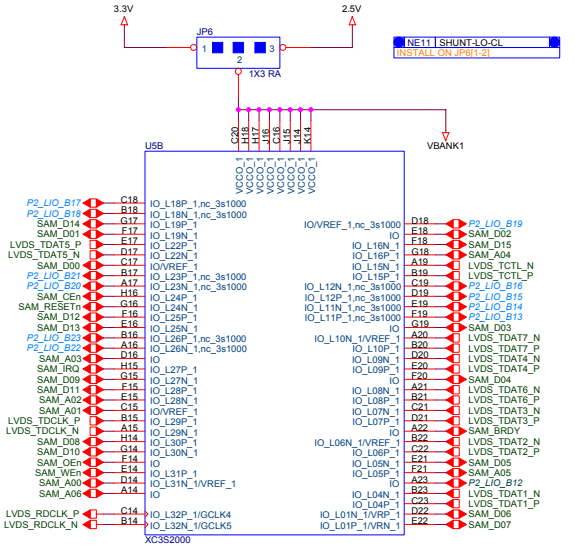
BANK 0 - JX2 & USB & RS232 & CLOCKs — JX3



62 IO **35 JX2** **1 CLOCK**
13 1500 **10 USB** **1 NC**
= 49 IO **2 RS232**

13 JX3

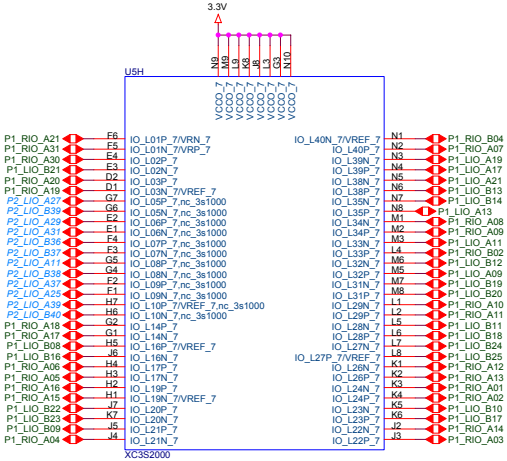
BANK 1 - SAM & LVDS — JX3



61 IO **29 SAM** **1 JX3**
11 1500 **18 LVDS TX**
= 50 IO **2 LVDS RX**

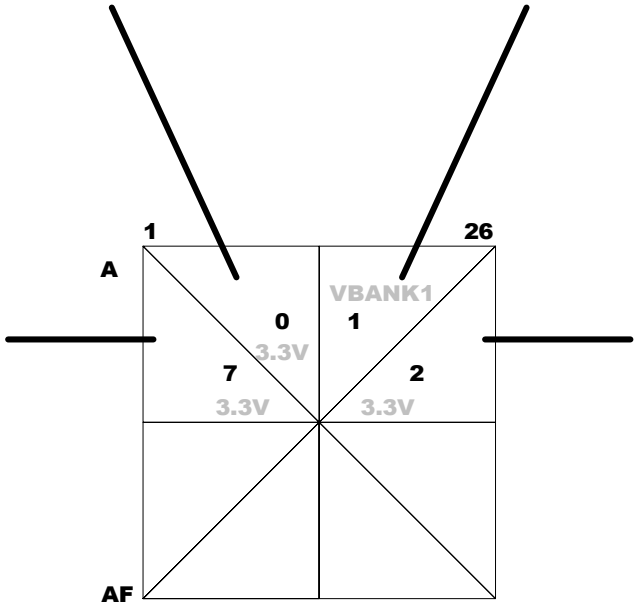
11 JX3

BANK 7 - JX1 & JX2 — JX3

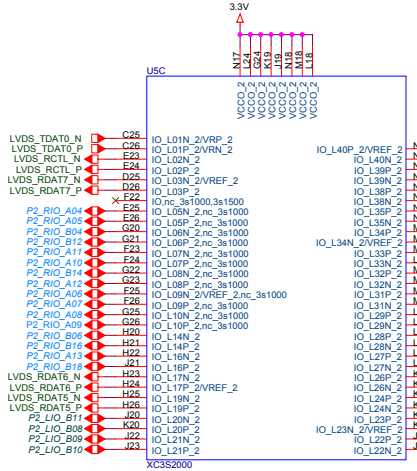


60 IO **23 JX1**
12 1500 **25 JX2**
= 48 IO

12 JX3



BANK 2 - LVDS & JX3 & JX4 — JX4



60 IO **2 LVDS TX** **4 JX3**
12 1500 **18 LVDS RX** **24 JX4**
= 48 IO

12 JX4

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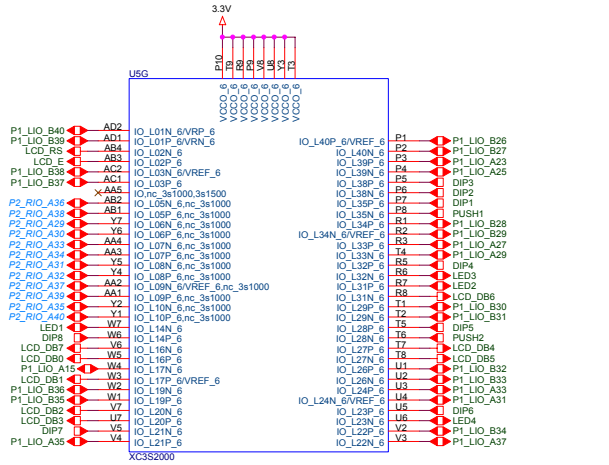
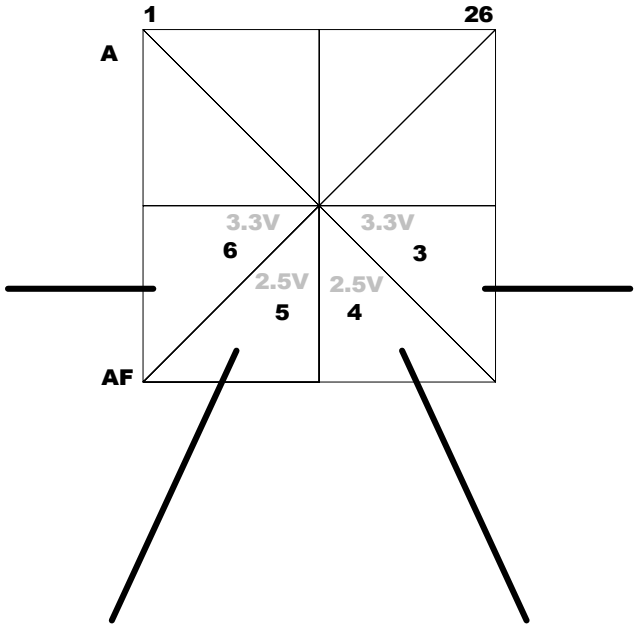
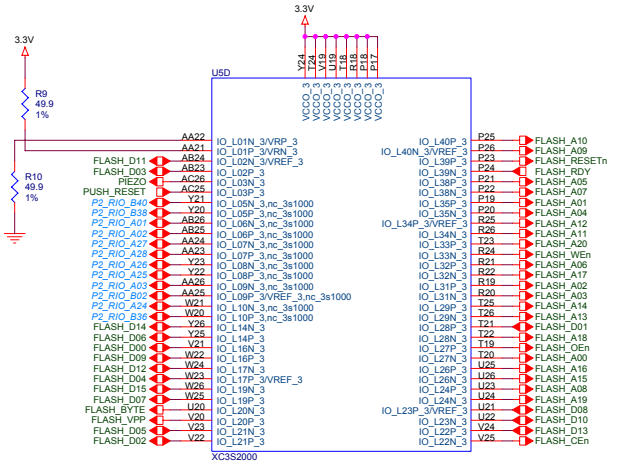
BANK 6 - JX1 & LCD & DIP & PUSH & LED — JX4



61 IO
12 1500 — 24 JX1 — 2 PUSH
1 2000 — 10 LCD — 4 LED — 12 JX4
= 48 IO — 8 DIP — 1 NC

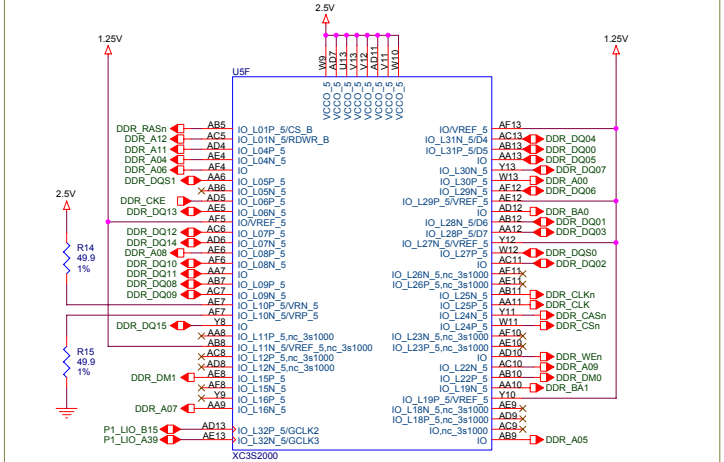


BANK 3 - FLASH & EEPROM & RESET — JX4



60 IO — 2 DCI — 1 RESET
12 1500 — 44 FLASH — 1 PIZEO
= 48 IO — 12 JX4

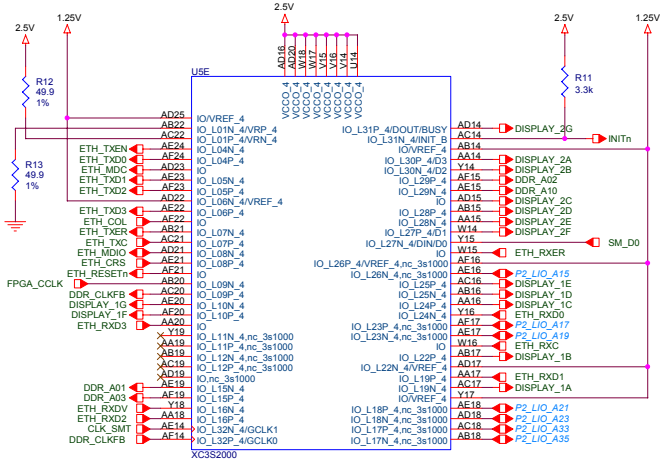
BANK 5 - DDR & JX1 — VREF & SSD



61 IO — 2 DCI — 38 DDR
11 1500 — 5 VREF — 2 JX1 (GCLKs)
= 50 IO — 3 NC — 1 VREF — 10 NC

BANK 4 - DDR & ETHERNET & JX3 — JX3 & VREF & SSD

NOTE: CLKFB MUST BE ON SAME SIDE AS CLKIN



63 IO
2 CONFIG — 2 DCI — 14 SSD — 4 DDR — 1 VREF
13 1500 — 5 VREF — 19 ETHERNET — 1 CCLK OUTPUT — 7 JX3
= 48 IO — 2 DDR FB — 1 CLOCK — 5 NC

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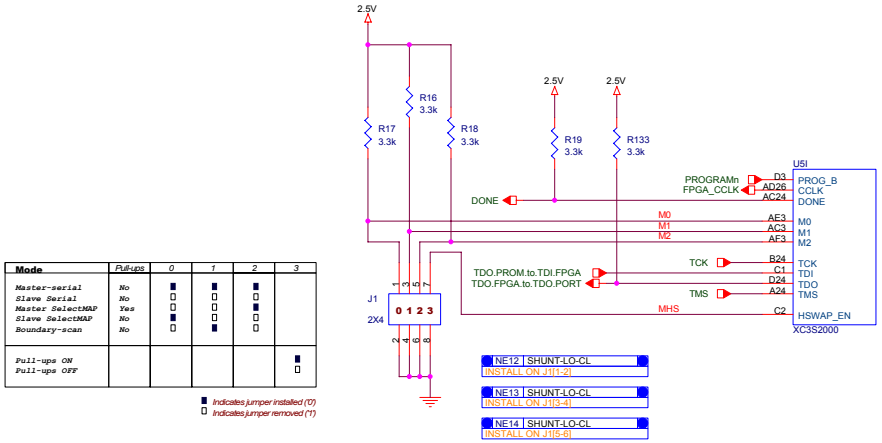
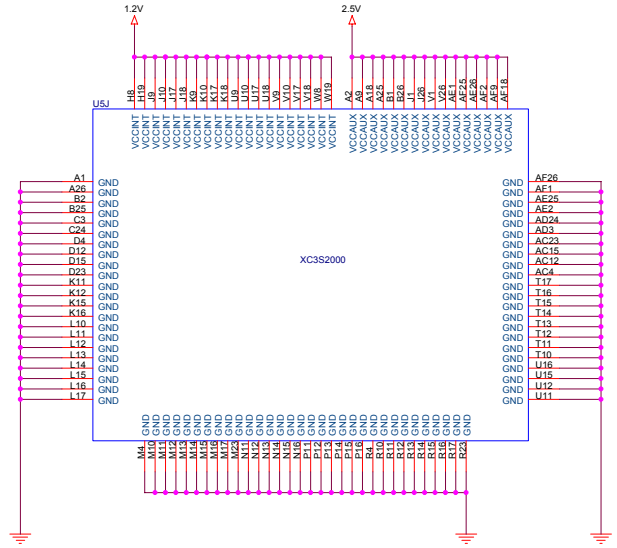
CONFIGURATION BLOCK

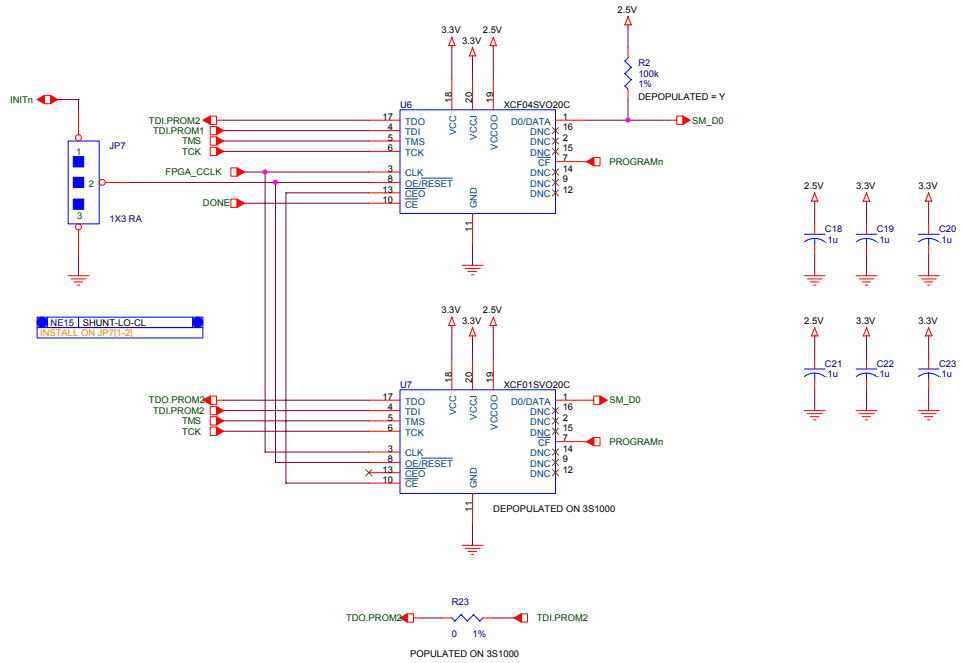


POWER BLOCK

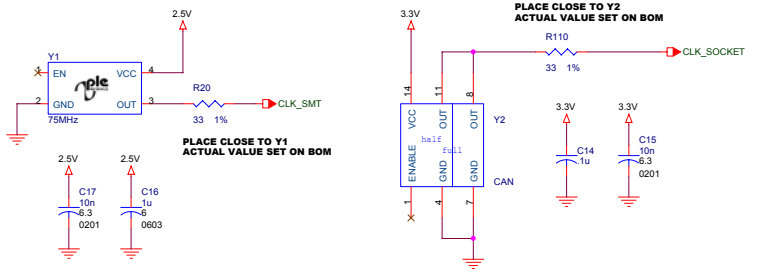


Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: SPARTAN 3 MB BOARD	PAGE TITLE: FPGA AUX	LAST MODIFIED: Monday, May 31, 2004	SIZE: C	DESIGNER: JBE	REVISION: 2	SHEET: 6 of 15

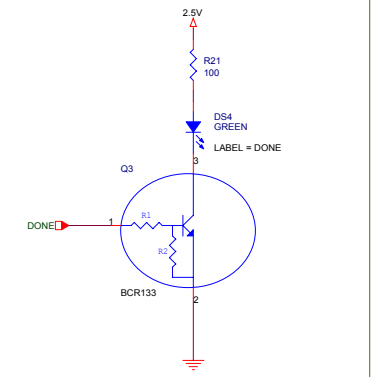
PROM (PLATFORM FLASH)



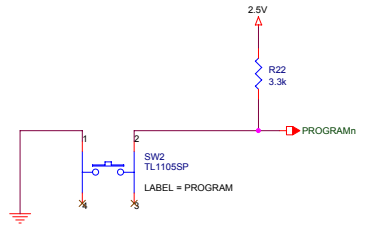
CLOCKs



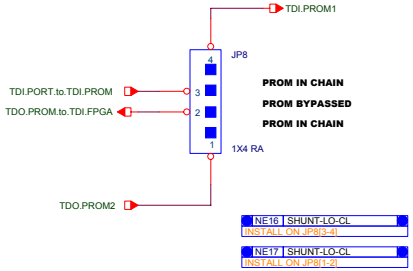
DONE LED



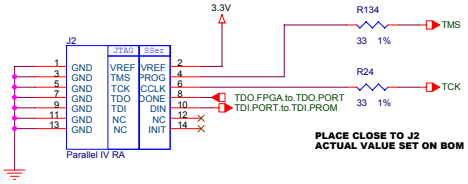
PROGRAM PUSHBUTTON



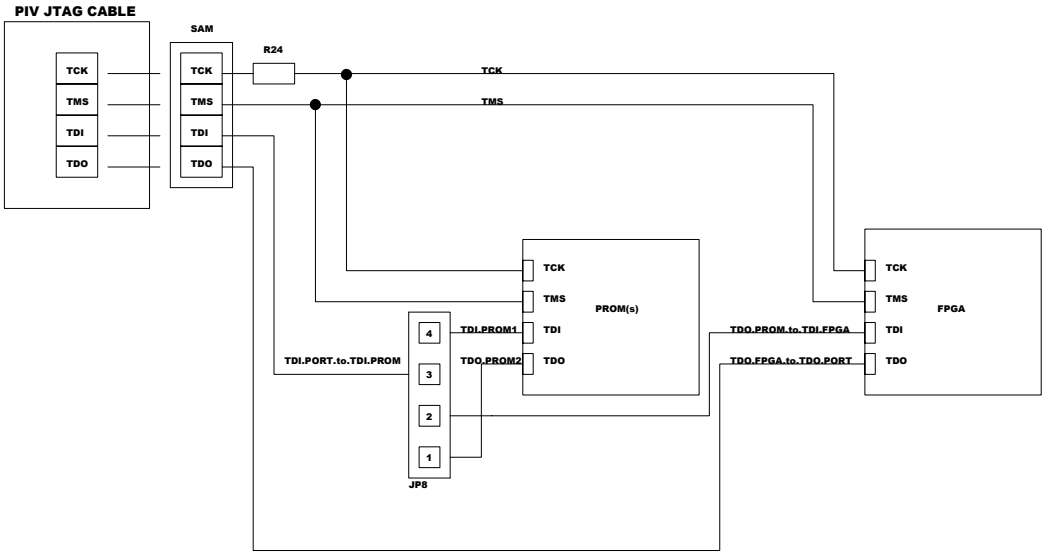
PROM JTAG BYPASS



JTAG PORT

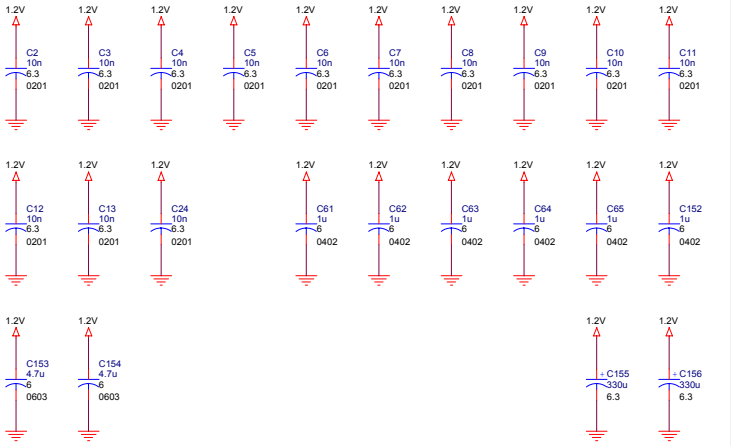


JTAG CONNECTION DIAGRAM

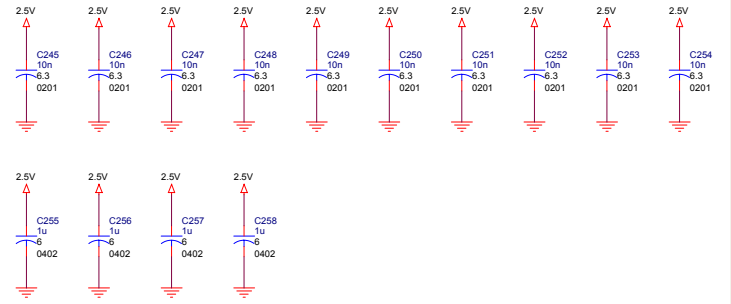


MemecBoard Calgary, Alberta Canada	BOARD TITLE: SPARTAN 3 MB BOARD	PAGE TITLE: FPGA PERIPHERALS	LAST MODIFIED: Monday, May 31, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	7	of	15

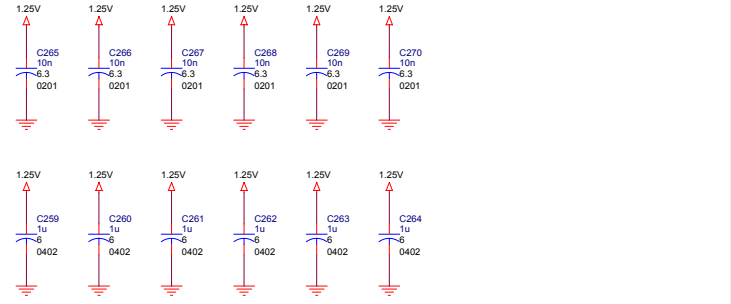
FPGA CORE DECOUPLING (20 pins)



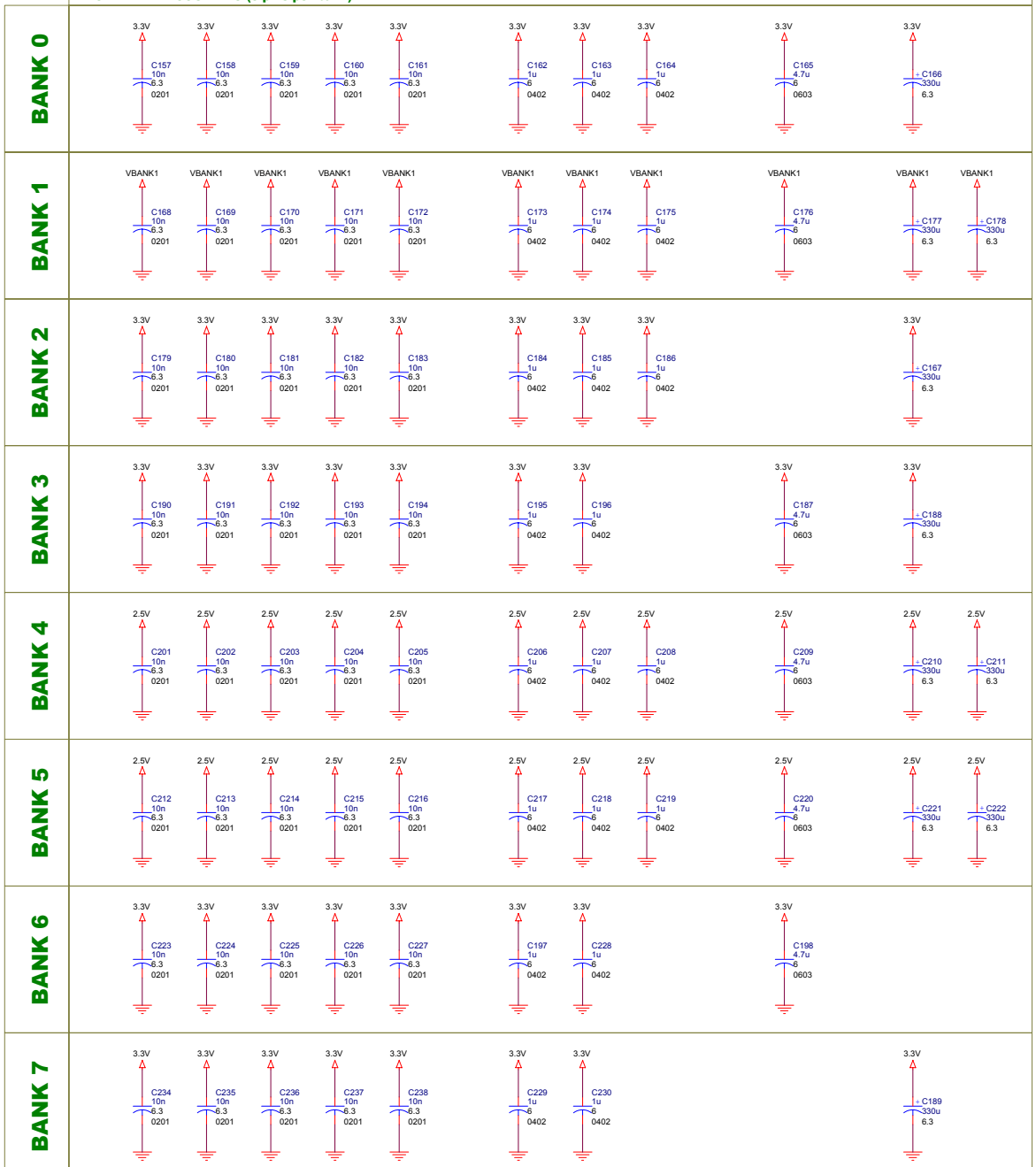
FPGA AUX DECOUPLING (16 pins)



VREF DECOUPLING (12 pins)

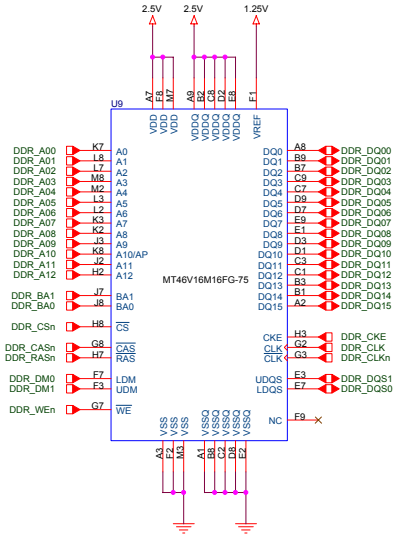


FPGA BANK DECOUPLING (8 pins per bank)

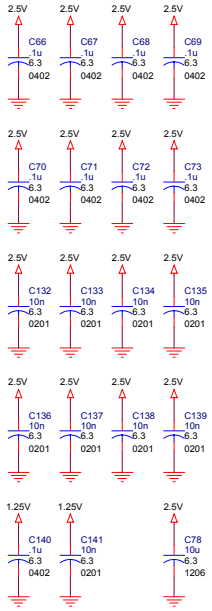


MemecBoard Calgary, Alberta Canada	BOARD TITLE: SPARTAN 3 MB BOARD	PAGE TITLE: FPGA DECOUPLING	LAST MODIFIED: Monday, May 31, 2004	SIZE: C	DESIGNER: JBE	REVISION: 2	SHEET: 8 of 15

DDR LOWER (LSB)

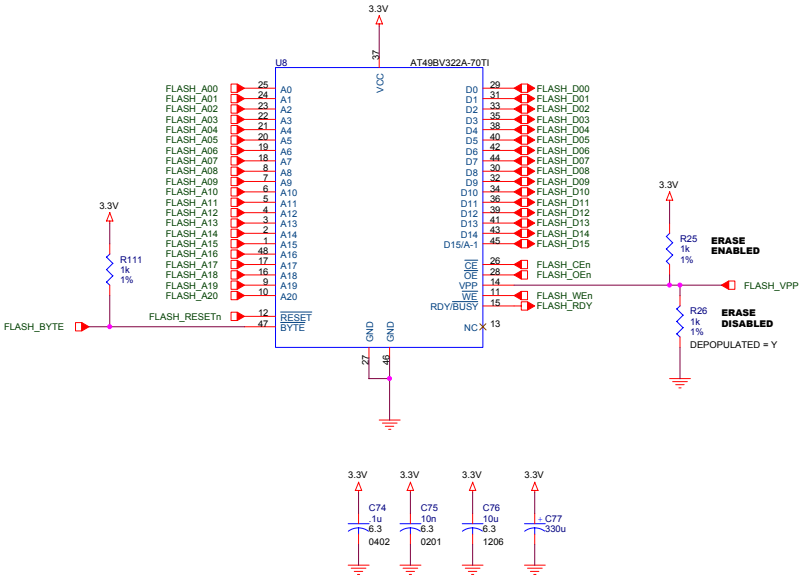


DECOUPLING



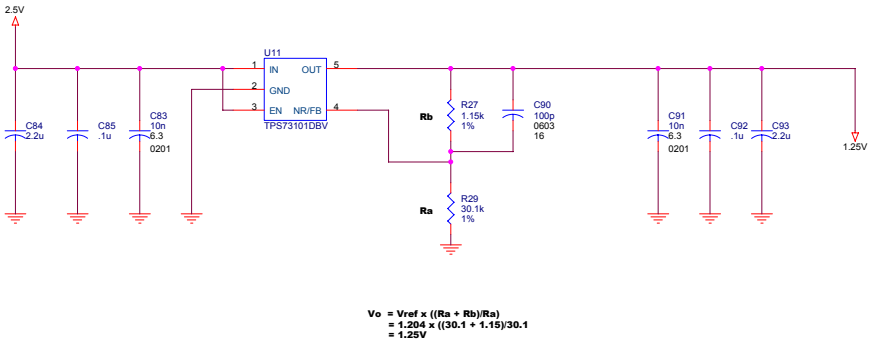
42 IO

FLASH



42 IO

1.25V



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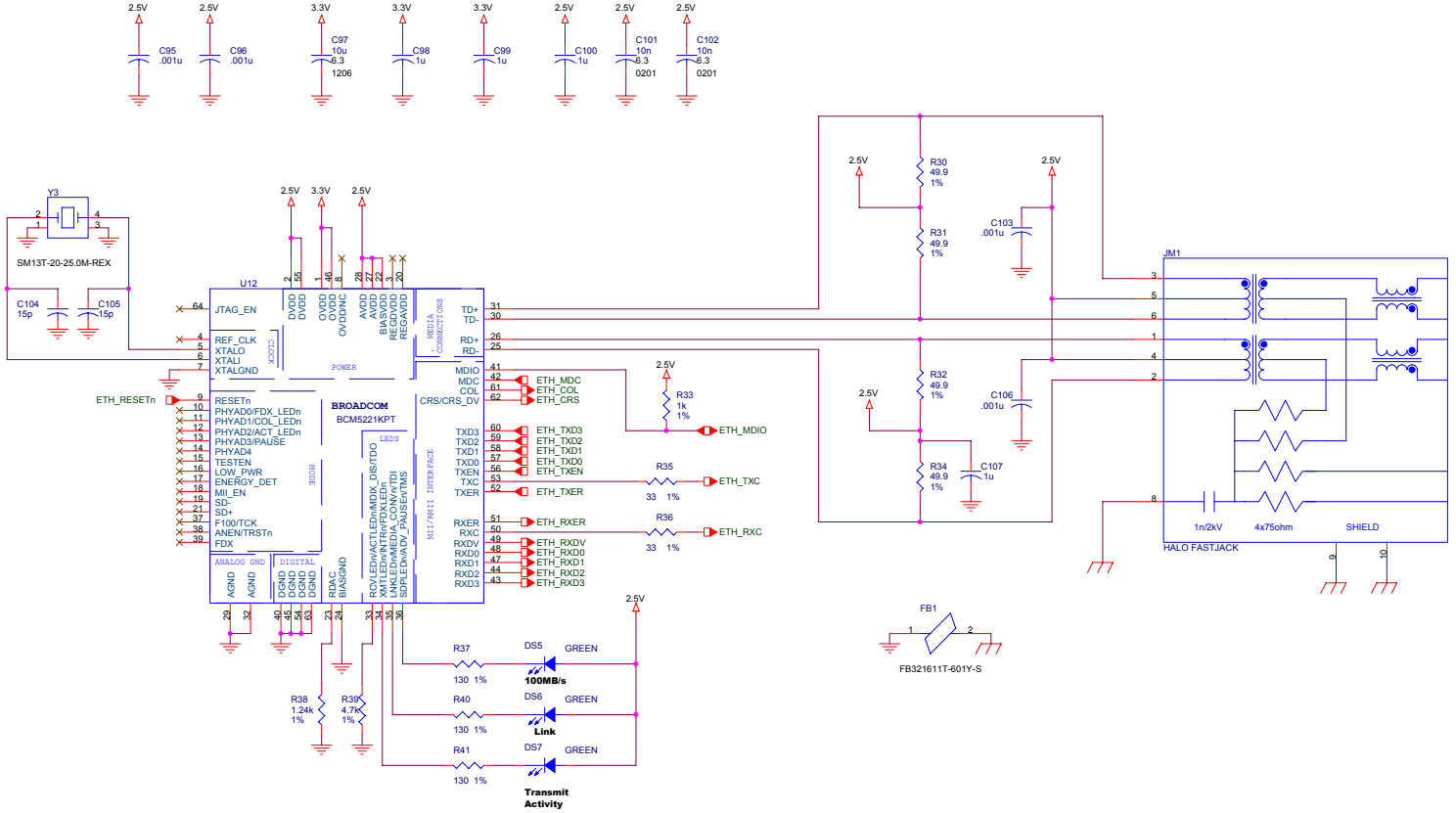
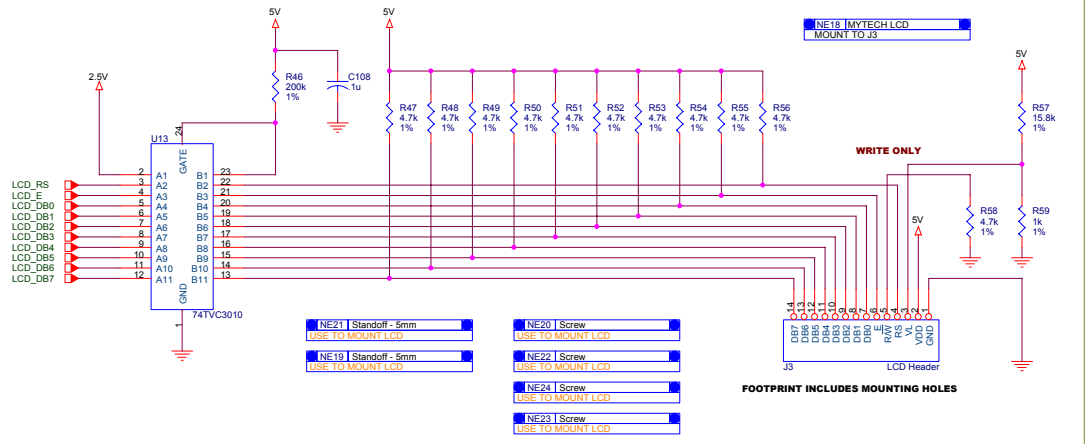
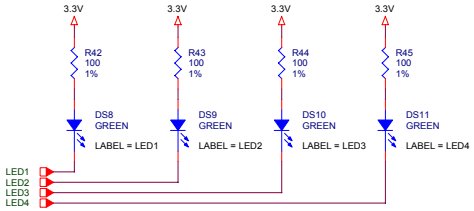


Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE SPARTAN 3 MB BOARD	PAGE TITLE ETHERNET PHY	LAST MODIFIED Wednesday, June 02, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	10	of	15

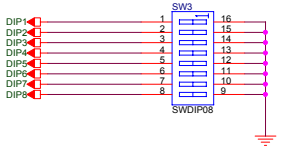
LCD MODULE CONNECTOR



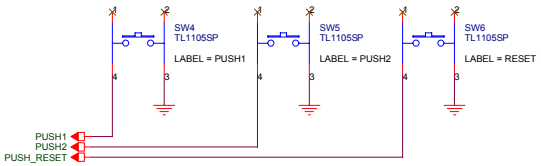
LEDs



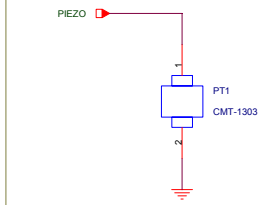
DIP SWITCH



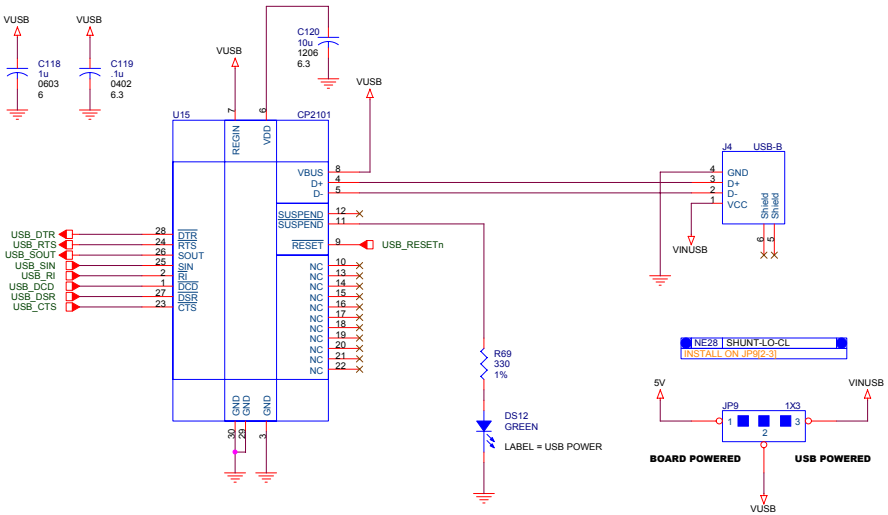
PUSHBUTTONS



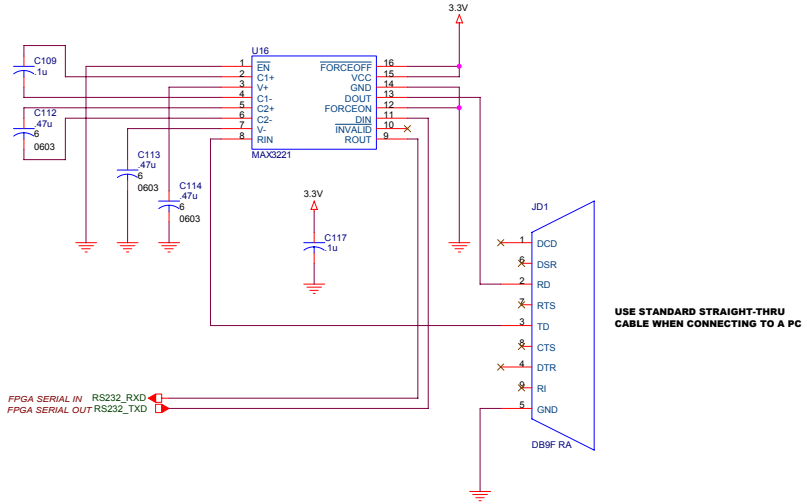
PIEZO



USB

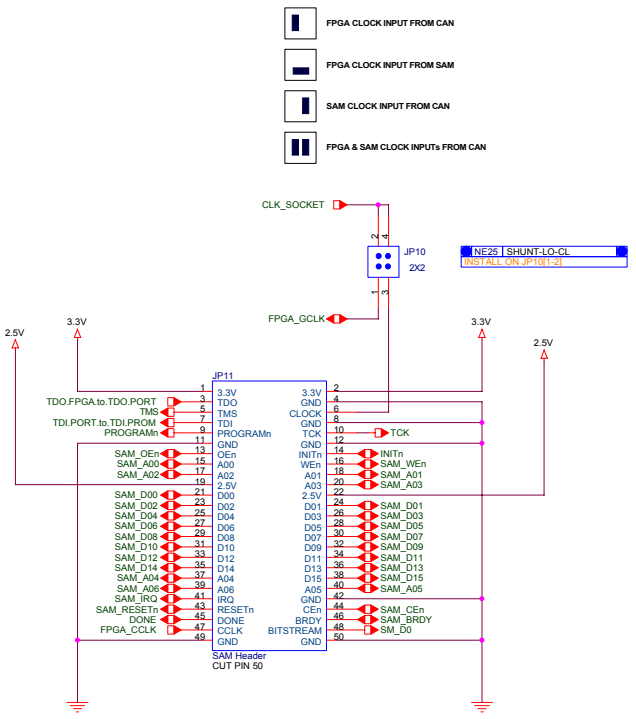


SERIAL PORT

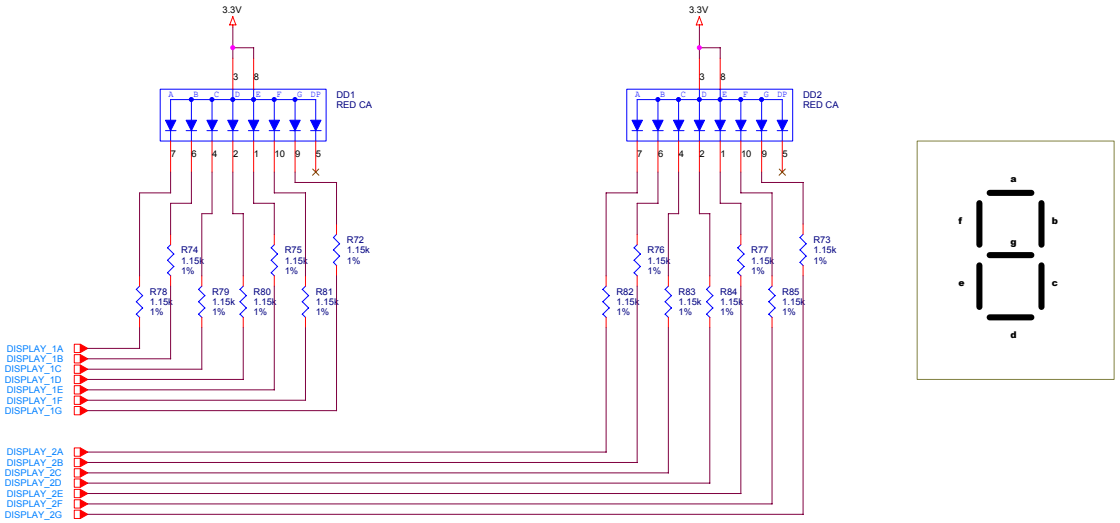


MemecBoard Calgary, Alberta Canada	BOARD TITLE: SPARTAN 3 MB BOARD	PAGE TITLE: USER IO	LAST MODIFIED: Wednesday, June 02, 2004	SIZE: C	DESIGNER: JBE	REVISION: 2	SHEET: 11 of 15

SYSTEM ACE MODULE



SEVEN SEGMENT DISPLAYs



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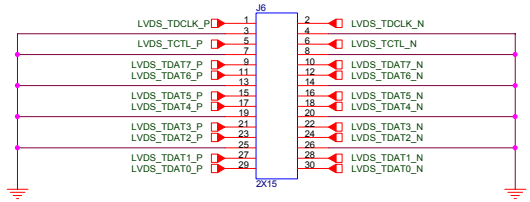
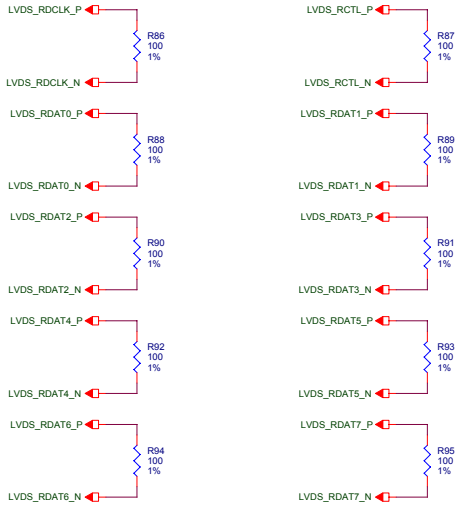
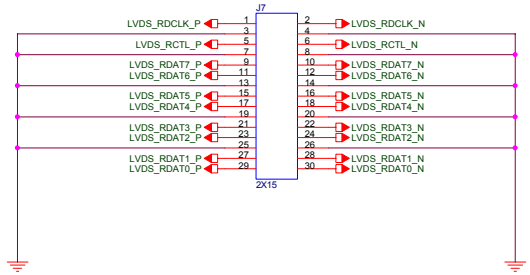
LVDS TRANSMIT

No transmit termination required for Spartan 3



LVDS RECEIVE





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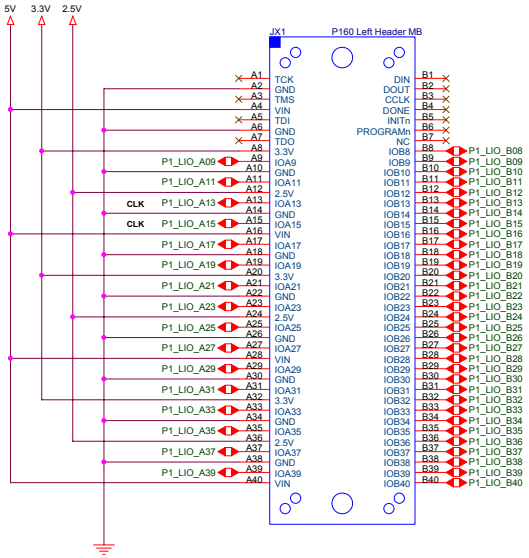
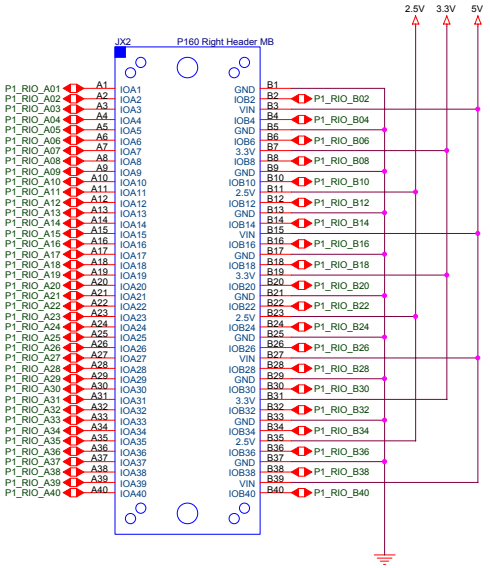
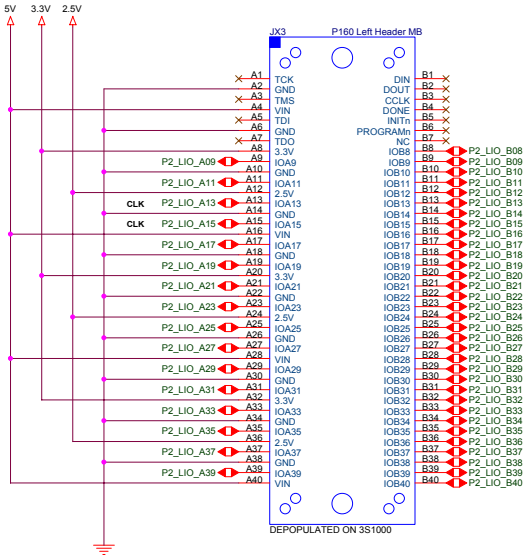
P160 #1

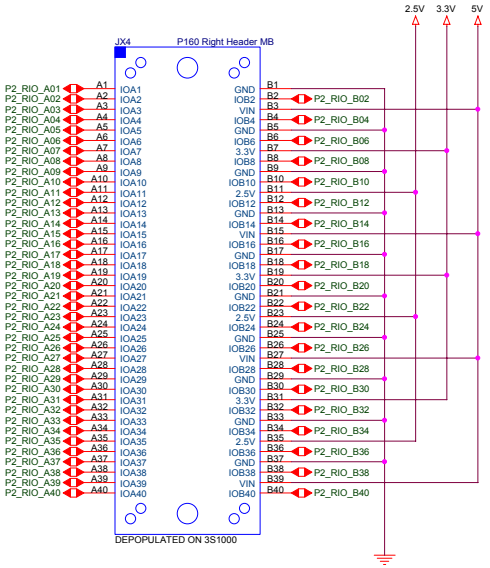




P160 #2



3S1500 & 3S2000 ONLY



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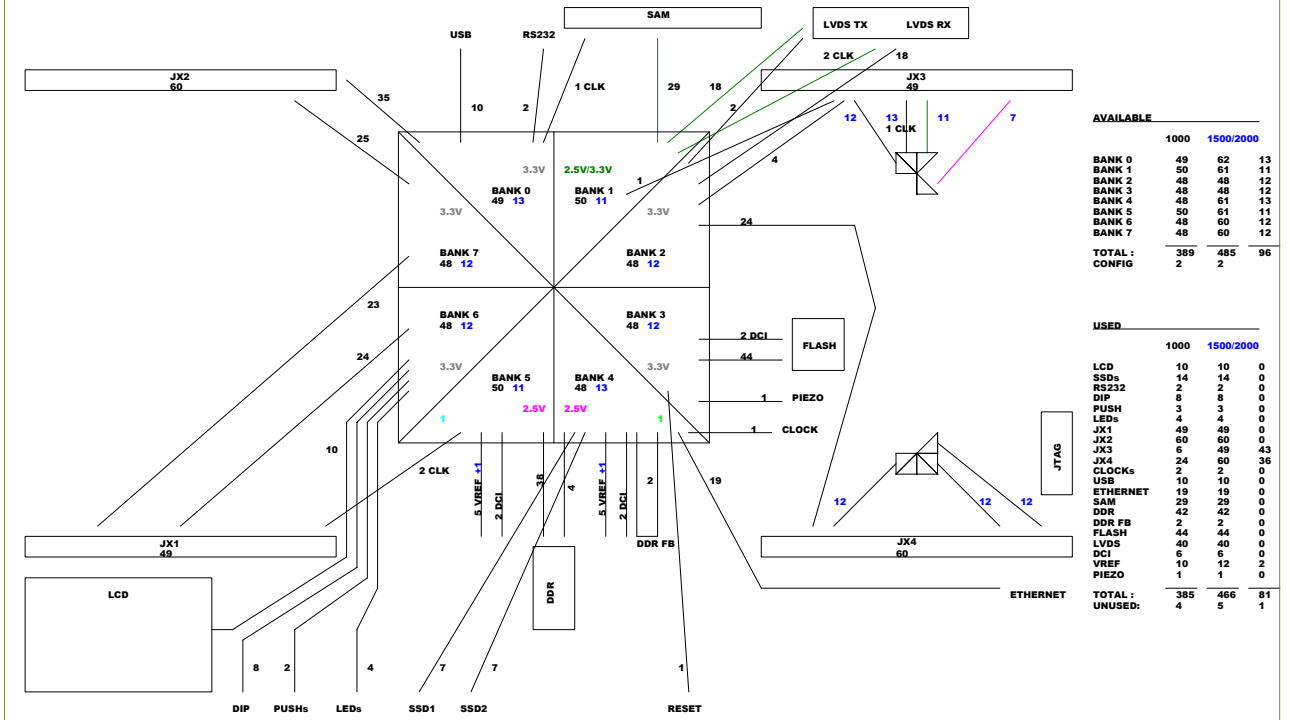
REV A	REV 1	REV 1.1	REV 2
CHANGED USB FROM TI TO CYGNAL	CHANGED R107 PART NUMBER	REVERSED R27 & R29 VALUES	
ADDED ASSEMBLY NOTES	CHANGED C278 & C291 TO 0.047uF Y5R	MADE ALL P160 SIGNAL NAMES TWO DIGITS	
CHANGED CLOCK CAN FROM 100MHz TO 75MHz	CHANGED 7-SEG DISPLAY PART NUMBER	CORRECTED PIN COUNT DOCUMENTATION ON FPGA BLOCKS	
CORRECTED VOLTAGE ON DCI RESISTOR ON BANK 3	CHANGED 7-SEG RESISTORS FROM 100 TO 1.15k	CHANGED DDR PART NUMBER TO MICRON	
MOVED THREE ETHERNET SIGNALS FROM BANK3 TO BANK4	ADDED INDUCTOR NOTES	CHANGED JTAG CHAIN FROM 2.5V TO 3.3V	
ADDED FLASH BYTE AND VPP SIGNALS		CHANGED SECOND PROM FROM 04 TO 01	
MOVED SSD SIGNALS TO BANK4 1000 PINS		CHANGED CASCADE ORDER OF PROMs	
ADDED PIEZO		REASSIGNED GCLK PINS TO JX1	
REPLACED 3.3V CIRCUIT WITH TPS40k		ADDED CCLK CONNECTION	
REPLACED 2.5V CIRCUIT WITH TPS40k		REASSIGNED DDR SIGNALS AT FPGA	
CHANGED INDUCTOR AND FET IN 1.2V CIRCUIT			
ADJUSTED 1.2V RAIL FROM 1.35V TO 1.2V			
CHANGED 1.25V REGULATOR FROM TPS79101 TO TPS73101			
COMBINED TWO TLC SUPERVISORS INTO ONE TPS3806			
CHANGED POWER SEQUENCING TO 2.5V, 1.2V, 3.3V			
ADDED PULL-UPS TO VOLTAGE DISABLE JUMPERS			
REMOVED ONE DDR DEVICE (UPPER)			
CHANGED DDR PART NUMBER TO INFINEON			
REASSIGNED DDR SIGNALS			
MOVED DDR CLOCK FEEDBACK OUTPUT FROM BANK5 TO BANK4			

PLACEMENT



AVAILABLE

	1000	1500/2000	
BANK 0	49	62	13
BANK 1	50	61	11
BANK 2	48	48	12
BANK 3	48	48	12
BANK 4	48	61	13
BANK 5	50	61	11
BANK 6	48	60	12
BANK 7	48	60	12
TOTAL :	389	485	96
CONFIG	2	2	

USED

	1000	1500/2000	
LCD	10	10	0
SSDs	14	14	0
RS232	2	2	0
DIP	8	8	0
PUSH	3	3	0
LEDs	4	4	0
JX1	49	49	0
JX2	60	60	0
JX3	6	49	43
JX4	24	60	36
CLOCKs	2	2	0
USB	10	10	0
ETHERNET	19	19	0
SAM	29	29	0
DDR	42	42	0
DDR FB	2	2	0
FLASH	44	44	0
LVDS	40	40	0
DCI	6	6	0
VREF	10	12	2
PIEZO	1	1	0
TOTAL :	385	466	81
UNUSED:	4	5	1

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