Xilinx Virtex-5 LX Board

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10/11/06

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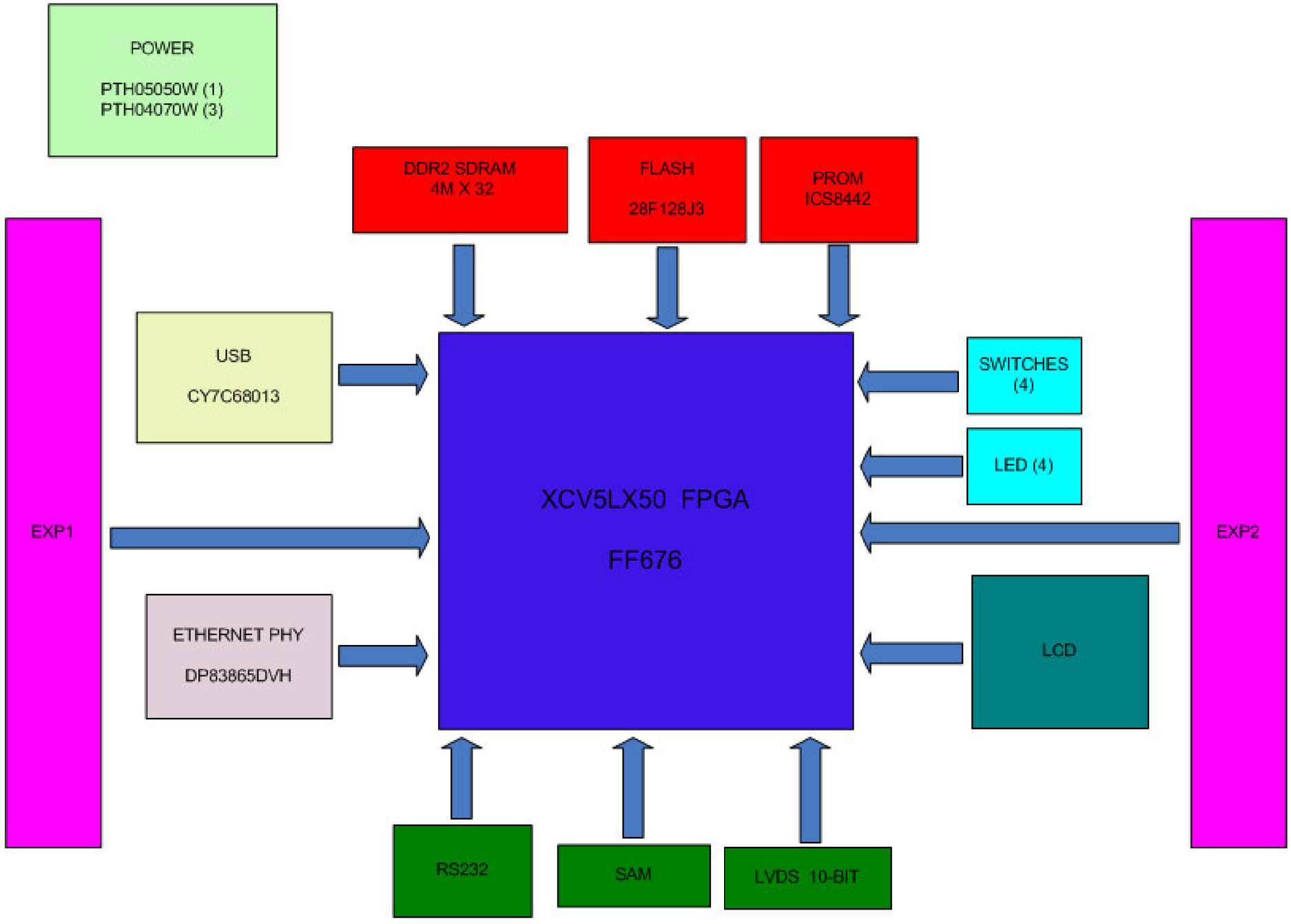
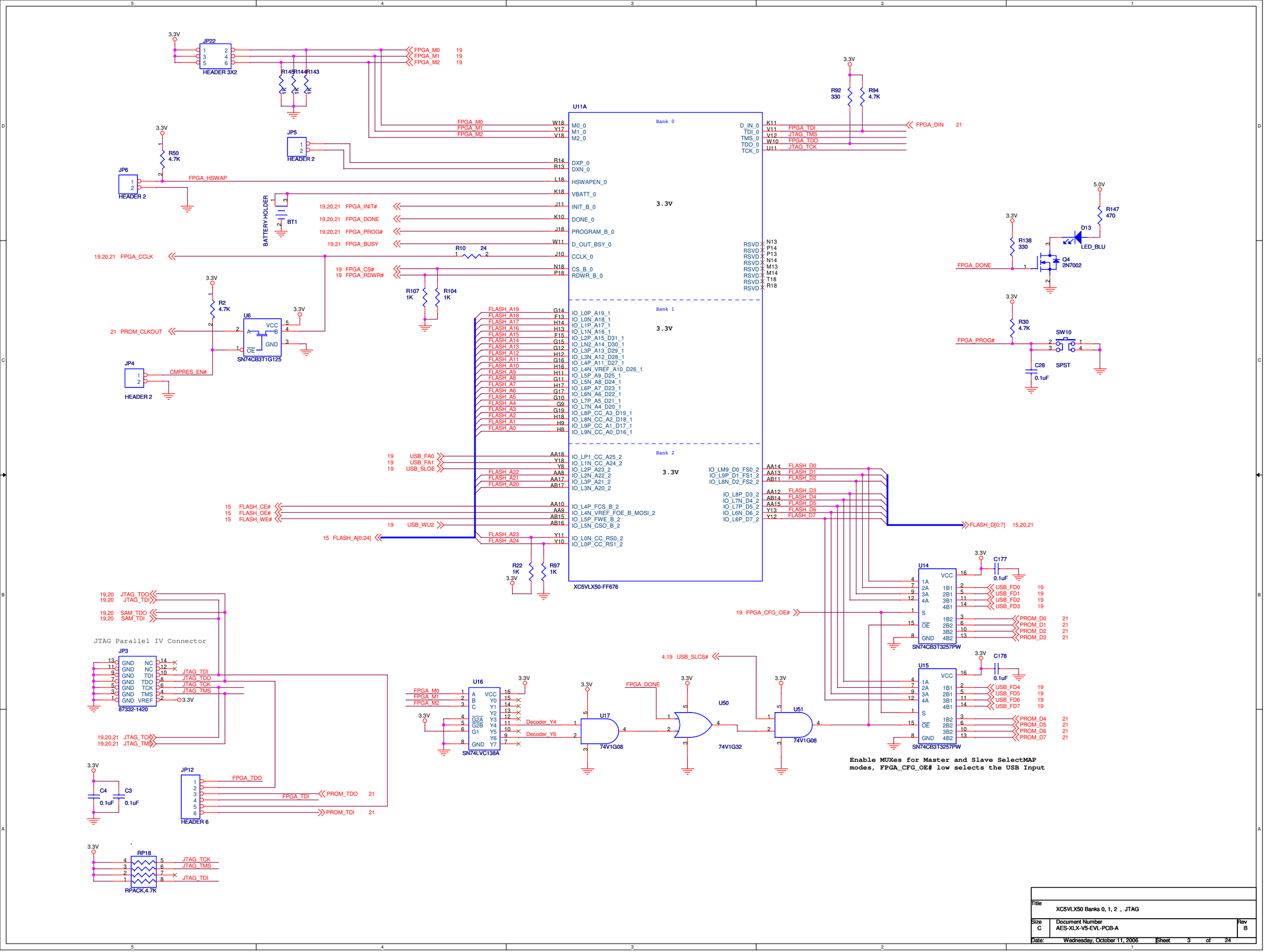
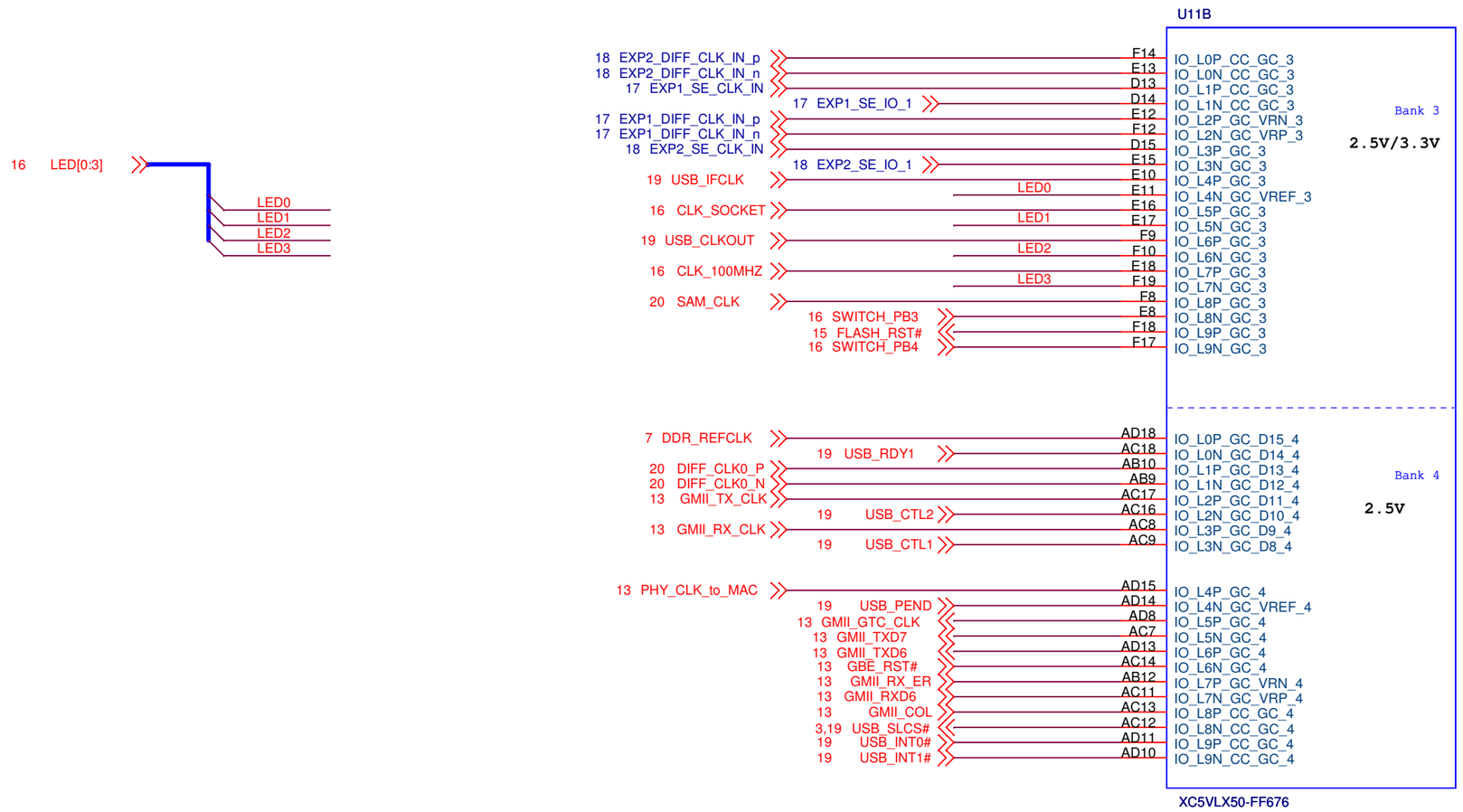
Title: Xilinx Virtex-5 LX Board	Lead Sheet	
Size: B	Document Number: AES-XLX-V5LX-SCH	Rev: B
Date: Wednesday, October 11, 2006	Sheet 1 of 24	

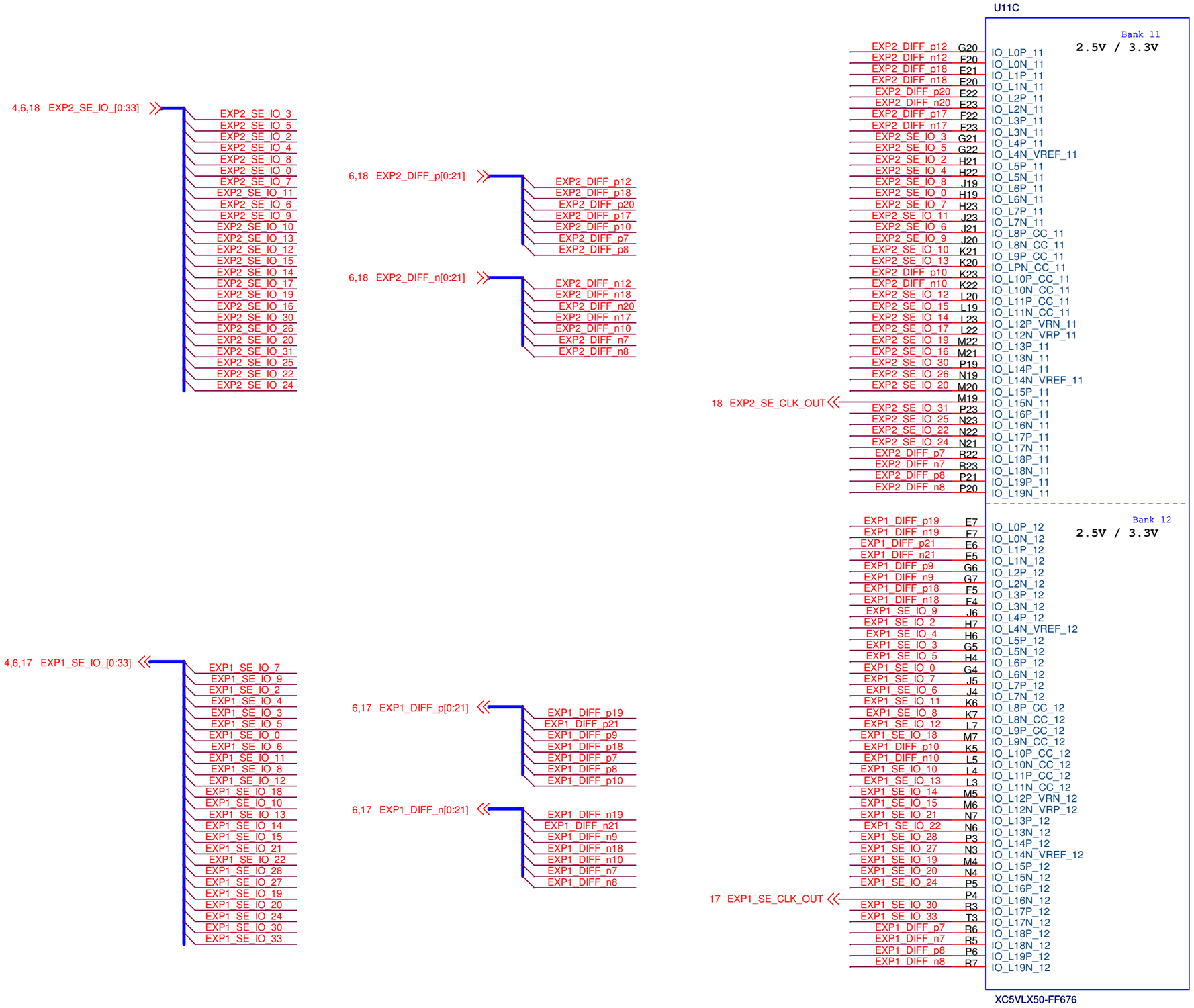


Title	Block Diagram	
Size A	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Wednesday, October 04, 2006	Sheet 2 of 24	

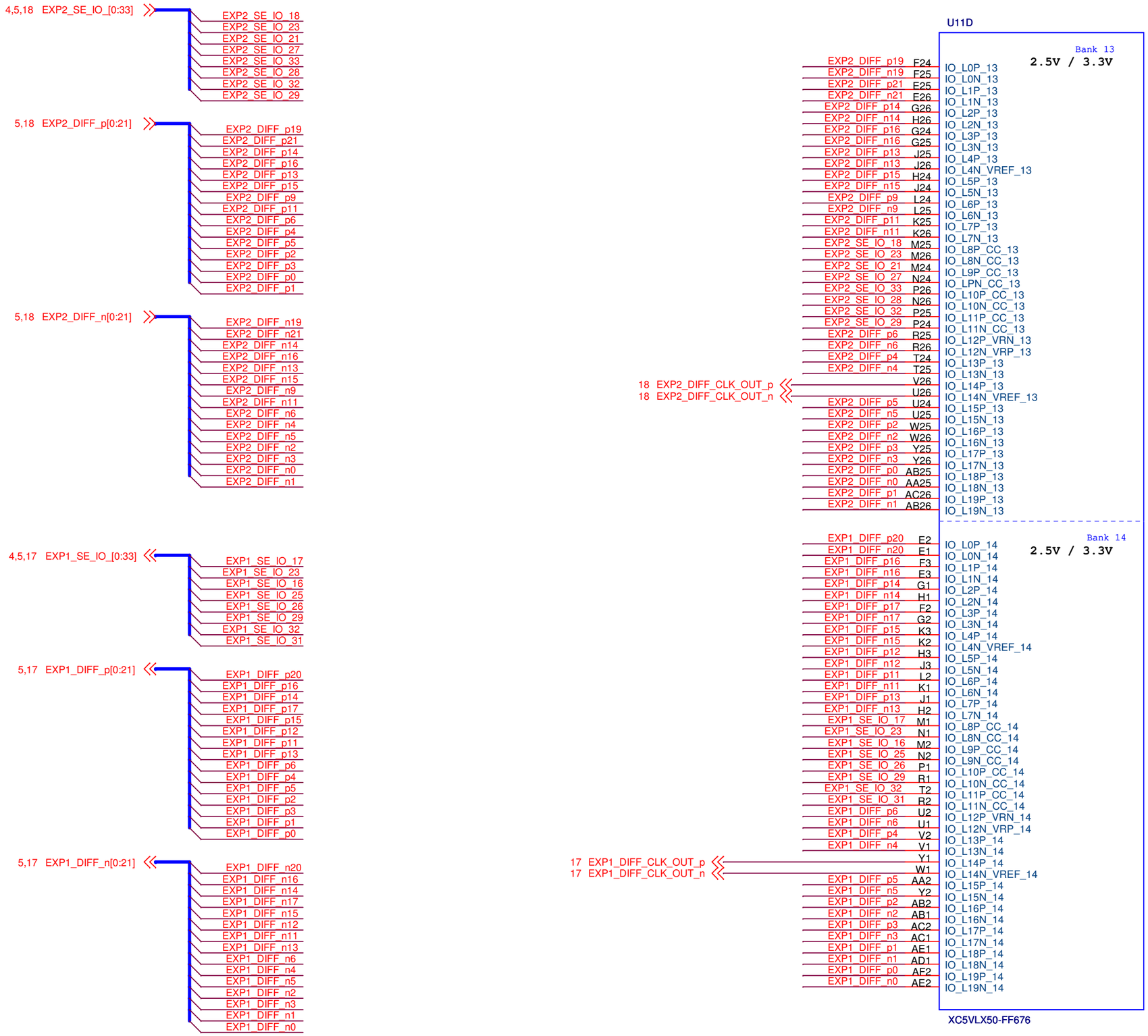

JP22
HEADER 3X2
FPGA_M0 19
FPGA_M1 19
FPGA_M2 19
R145 R144 R143
JP5
HEADER 2
JP6
HEADER 2
FPGA_HSWAP
R50 4.7K
BATTERY HOLDER
BT1
19,20,21 FPGA_CCLK
19,20,21 FPGA_INIT#
19,20,21 FPGA_DONE
19,20,21 FPGA_PROG#
19,21 FPGA_BUSY
19 FPGA_CS#
19 FPGA_RDWR#
R10 24
R107 1K
R104 1K
R2 4.7K
U6
SN74CB3T1G125
21 PROM_CLKOUT
JP4
HEADER 2
CMPRES_EN#
U11A
XC5VLX50-FF676
Bank 0
Bank 1
Bank 2
3.3V
M0_0 W18
M1_0 Y17
M2_0 V18
DXP_0 R14
DXN_0 R13
HSWAPEN_0 L18
VBATT_0 K18
INIT_B_0 J11
DONE_0 K10
PROGRAM_B_0 J18
D_OUT_BSY_0 W11
CCLK_0 J10
CS_B_0 N18
RDWR_B_0 P18
D_IN_0 K11 FPGA_TDI
TDI_0 V11 JTAG_TMS
TMS_0 V12 FPGA_TDO
TDO_0 W10 JTAG_TCK
TCK_0 U11
FPGA_DIN 21
RSVD N13
RSVD P14
RSVD P13
RSVD N14
RSVD M13
RSVD M14
RSVD T18
RSVD R18
FLASH_A19 G14 IO_L0P_A19_1
FLASH_A18 F13 IO_L0N_A18_1
FLASH_A17 H14 IO_L1P_A17_1
FLASH_A16 H13 IO_L1N_A16_1
FLASH_A15 F15 IO_L2P_A15_D31_1
FLASH_A14 G15 IO_L2N_A14_D30_1
FLASH_A13 G12 IO_L3P_A13_D29_1
FLASH_A12 H12 IO_L3N_A12_D28_1
FLASH_A11 G16 IO_L4P_A11_D27_1
FLASH_A10 H16 IO_L4N_VREF_A10_D26_1
FLASH_A9 H11 IO_L5P_A9_D25_1
FLASH_A8 G11 IO_L5N_A8_D24_1
FLASH_A7 H17 IO_L6P_A7_D23_1
FLASH_A6 G17 IO_L6N_A6_D22_1
FLASH_A5 G10 IO_L7P_A5_D21_1
FLASH_A4 G9 IO_L7N_A4_D20_1
FLASH_A3 G19 IO_L8P_CC_A3_D19_1
FLASH_A2 H18 IO_L8N_CC_A2_D18_1
FLASH_A1 H9 IO_L9P_CC_A1_D17_1
FLASH_A0 H8 IO_L9N_CC_A0_D16_1
19 USB_FA0 AA18 IO_LP1_CC_A25_2
19 USB_FA1 Y18 IO_L1N_CC_A24_2
19 USB_SLOE Y8 IO_L2P_A23_2
FLASH_A22 AA8 IO_L2N_A22_2
FLASH_A21 AA17 IO_L3P_A21_2
FLASH_A20 AB17 IO_L3N_A20_2
15 FLASH_CE# AA10 IO_L4P_FCS_B_2
15 FLASH_OE# AA9 IO_L4N_VREF_FOE_B_MOSI_2
15 FLASH_WE# AB15 IO_L5P_FWE_B_2
19 USB_WU2 AB16 IO_L5N_CSO_B_2
15 FLASH_A[0:24]
FLASH_A23 Y11 IO_L0N_CC_RS0_2
FLASH_A24 Y10 IO_L0P_CC_RS1_2
IO_LM9_D0_FS0_2 AA14 FLASH_D0
IO_L9P_D1_FS1_2 AA13 FLASH_D1
IO_L8N_D2_FS2_2 AB11 FLASH_D2
IO_L8P_D3_2 AA12 FLASH_D3
IO_L7N_D4_2 AB14 FLASH_D4
IO_L7P_D5_2 AA15 FLASH_D5
IO_L6N_D6_2 Y13 FLASH_D6
IO_L6P_D7_2 Y12 FLASH_D7
FLASH_D[0:7] 15,20,21
R22 1K
R97 1K
R92 330
R94 4.7K
R147 470
D13
LED_BLU
R138 330
Q4 2N7002
FPGA_DONE
R30 4.7K
FPGA_PROG#
SW10
SPST
C28 0.1uF
JTAG Parallel IV Connector
JP3
87332-1420
19,20 JTAG_TDO
19,20 JTAG_TDI
19,20 SAM_TDO
19,20 SAM_TDI
19,20,21 JTAG_TCK
19,20,21 JTAG_TMS
JP12
HEADER 6
FPGA_TDO
FPGA_TDI
PROM_TDO 21
PROM_TDI 21
C4 0.1uF
C3 0.1uF
RP18
RPACK,4.7K
JTAG_TCK
JTAG_TMS
JTAG_TDI
U16
SN74LVC138A
Decoder_Y4
Decoder_Y6
U17
74V1G08
U50
74V1G32
U51
74V1G08
4,19 USB_SLCS#
U14
SN74CB3T3257PW
U15
SN74CB3T3257PW
19 FPGA_CFG_OE#
USB_FD0 19
USB_FD1 19
USB_FD2 19
USB_FD3 19
PROM_D0 21
PROM_D1 21
PROM_D2 21
PROM_D3 21
USB_FD4 19
USB_FD5 19
USB_FD6 19
USB_FD7 19
PROM_D4 21
PROM_D5 21
PROM_D6 21
PROM_D7 21
C177 0.1uF
C178 0.1uF
Enable MUXes for Master and Slave SelectMAP modes, FPGA_CFG_OE# low selects the USB Input
Title
XC5VLX50 Banks 0, 1, 2 , JTAG
Size C
Document Number AES-XLX-V5-EVL-PCB-A
Rev B
Date: Wednesday, October 11, 2006
Sheet 3 of 24



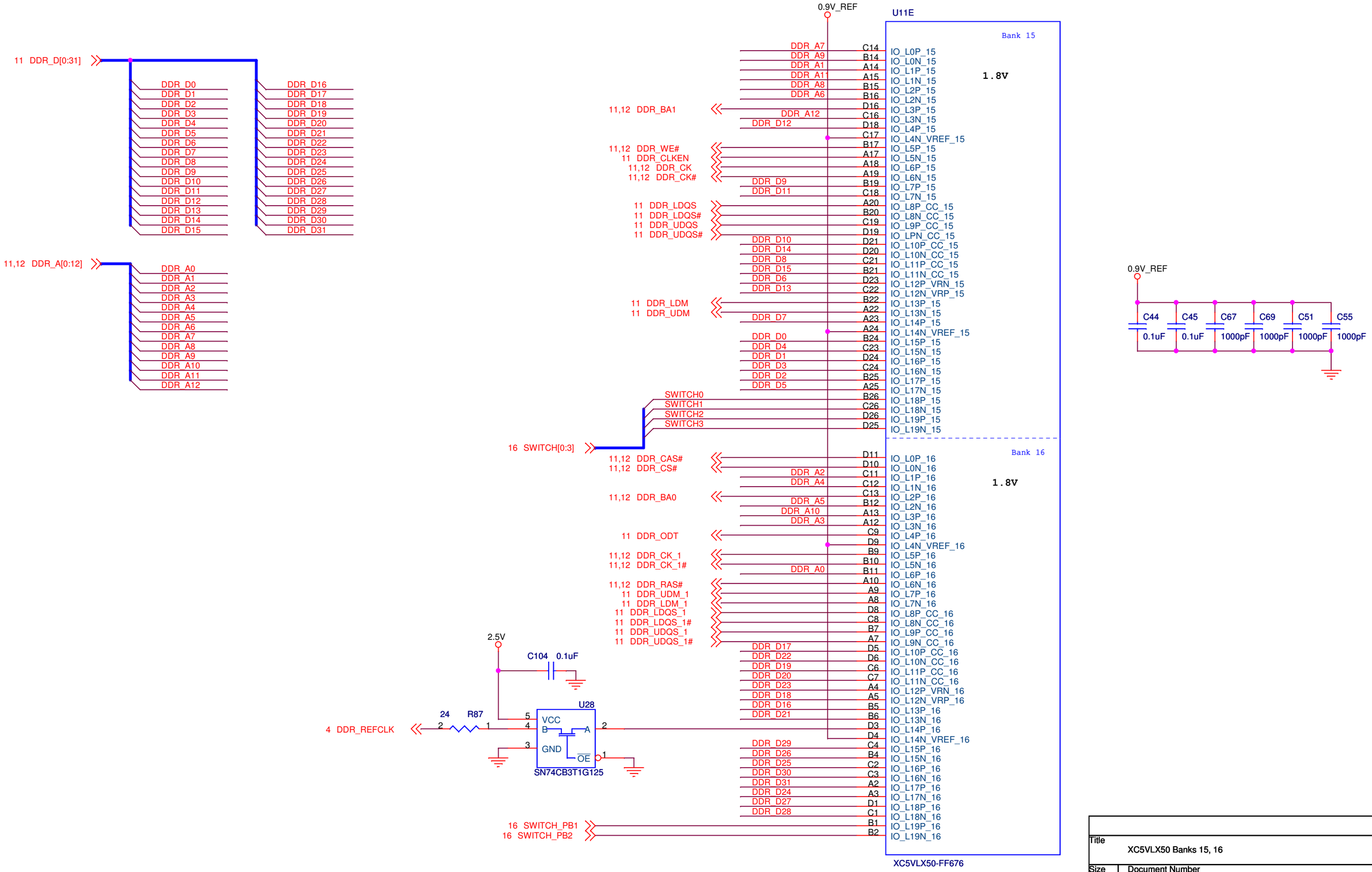
Title	XC5VLX50 Banks 3, 4		
Size B	Document Number AES-XLX-V5-EVL-PCB-A		Rev B
Date: Friday, October 06, 2006		Sheet 4 of 24	



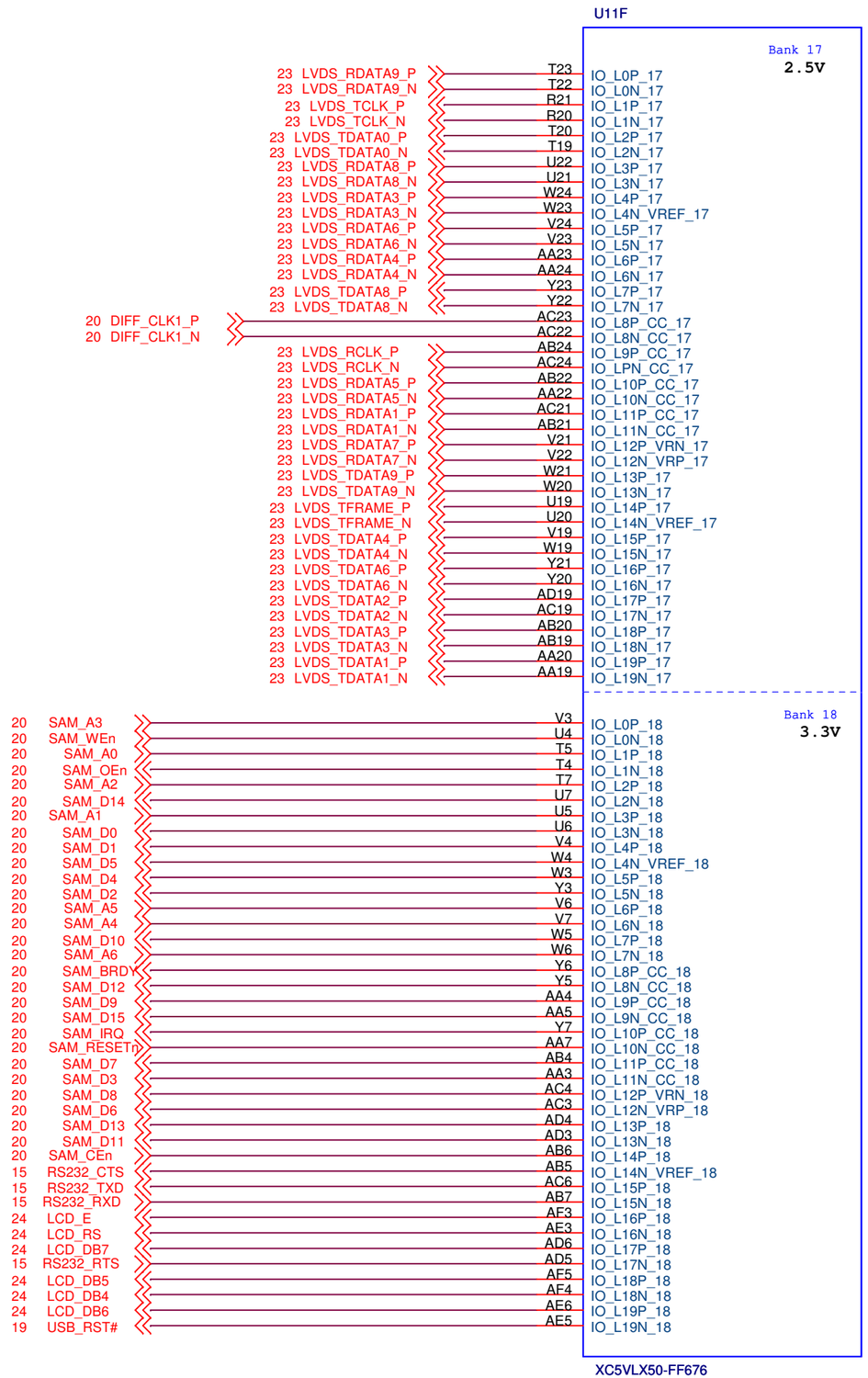
Title	XC5VLX50 Banks 11, 12		
Size B	Document Number AES-XLX-V5-EVL-PCB-A		Rev B
Date: Friday, October 06, 2006		Sheet 5 of 24	



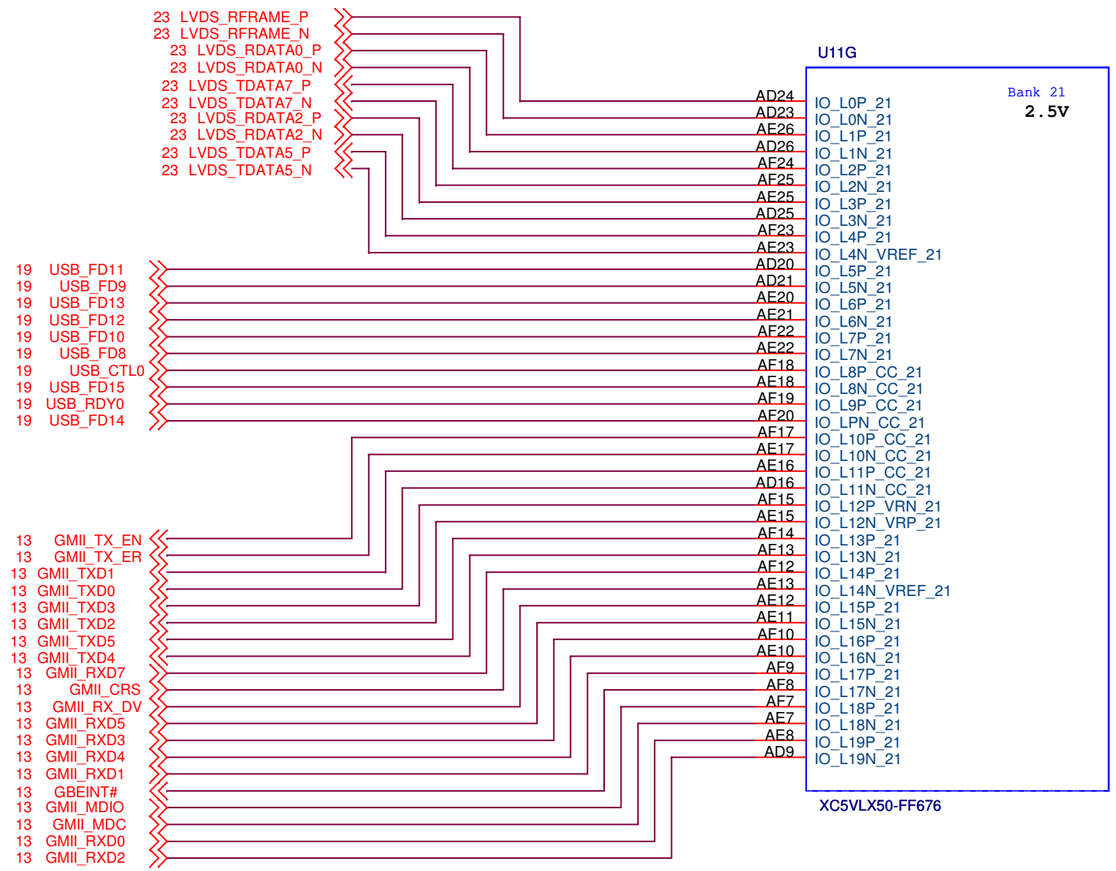
Title	XC5VLX50 Banks 13, 14	
Size B	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Friday, October 06, 2006	Sheet 6 of 24	



Title	XC5VLX50 Banks 15, 16	
Size B	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Friday, October 06, 2006	Sheet 7 of 24	



Title	XC5VLX50 Banks 17, 18	
Size B	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Friday, October 06, 2006	Sheet 8 of 24	



Title	XC5VLX50 Bank 21	
Size B	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
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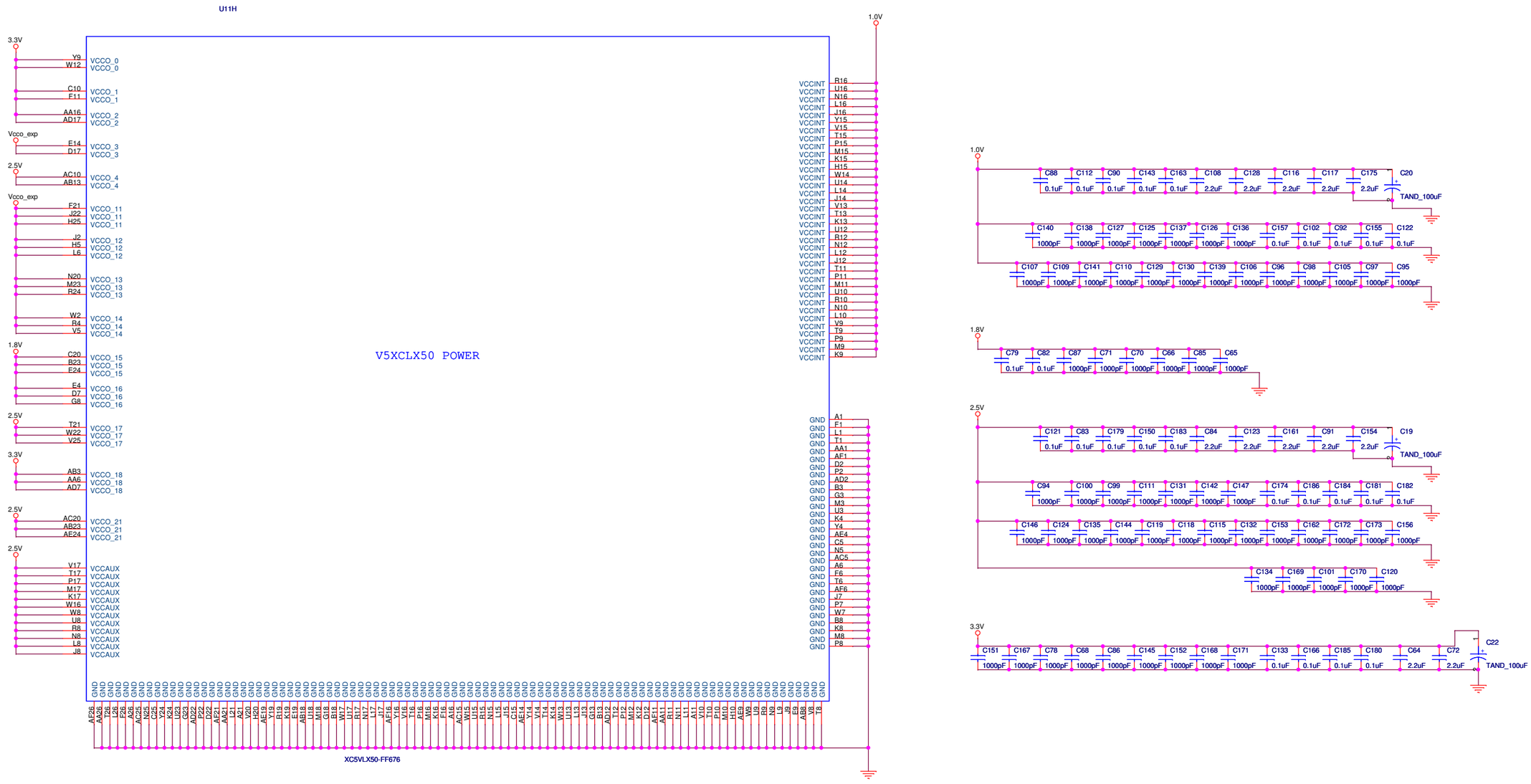
U11H
V5XCLX50 POWER
XC5VLX50-FF676
3.3V
Vcco_exp
2.5V
1.8V
1.0V
VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCO_4
VCCO_11
VCCO_12
VCCO_13
VCCO_14
VCCO_15
VCCO_16
VCCO_17
VCCO_18
VCCO_21
VCCAUX
VCCINT
GND
C20
C19
C22
TAND_100uF
C65
C120
C122
C182
C156
C64
C72
C95
C101
C107
C109
C110
C112
C116
C117
C121
C123
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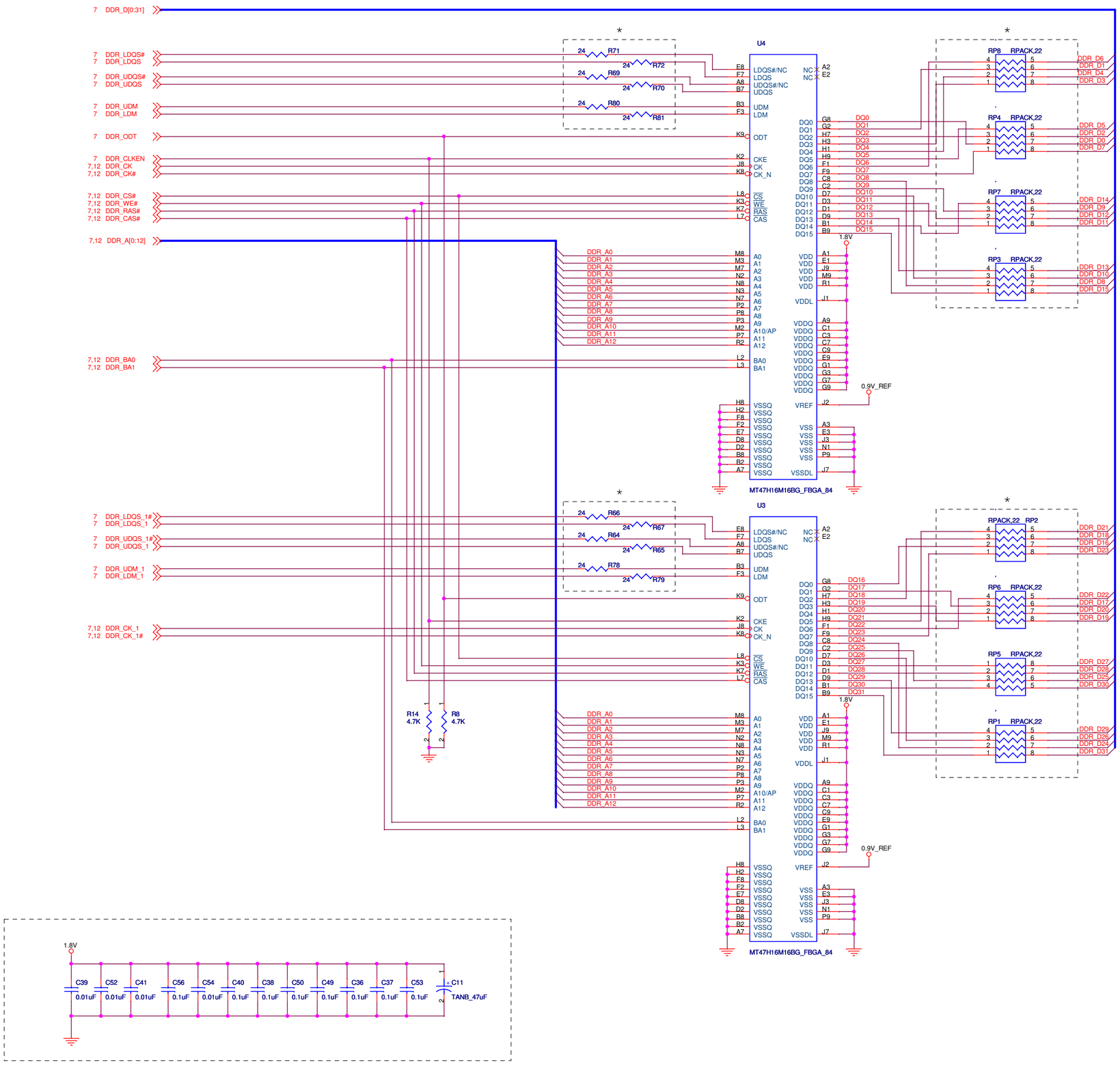
C210



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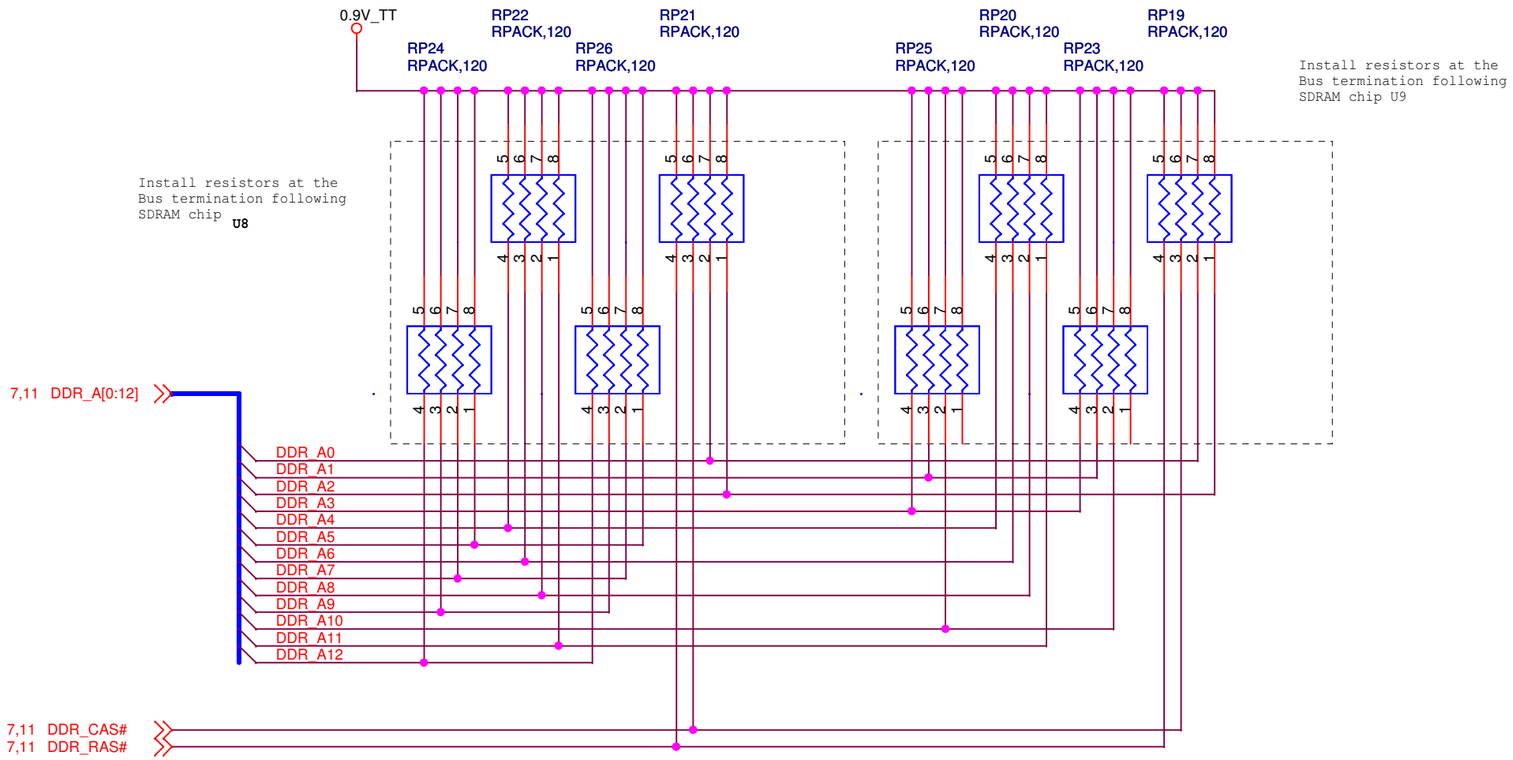
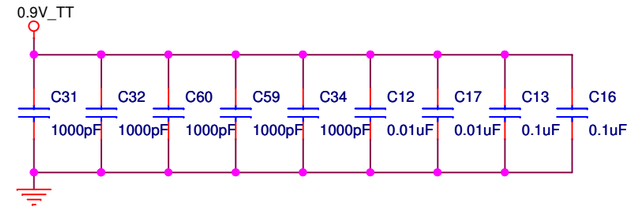
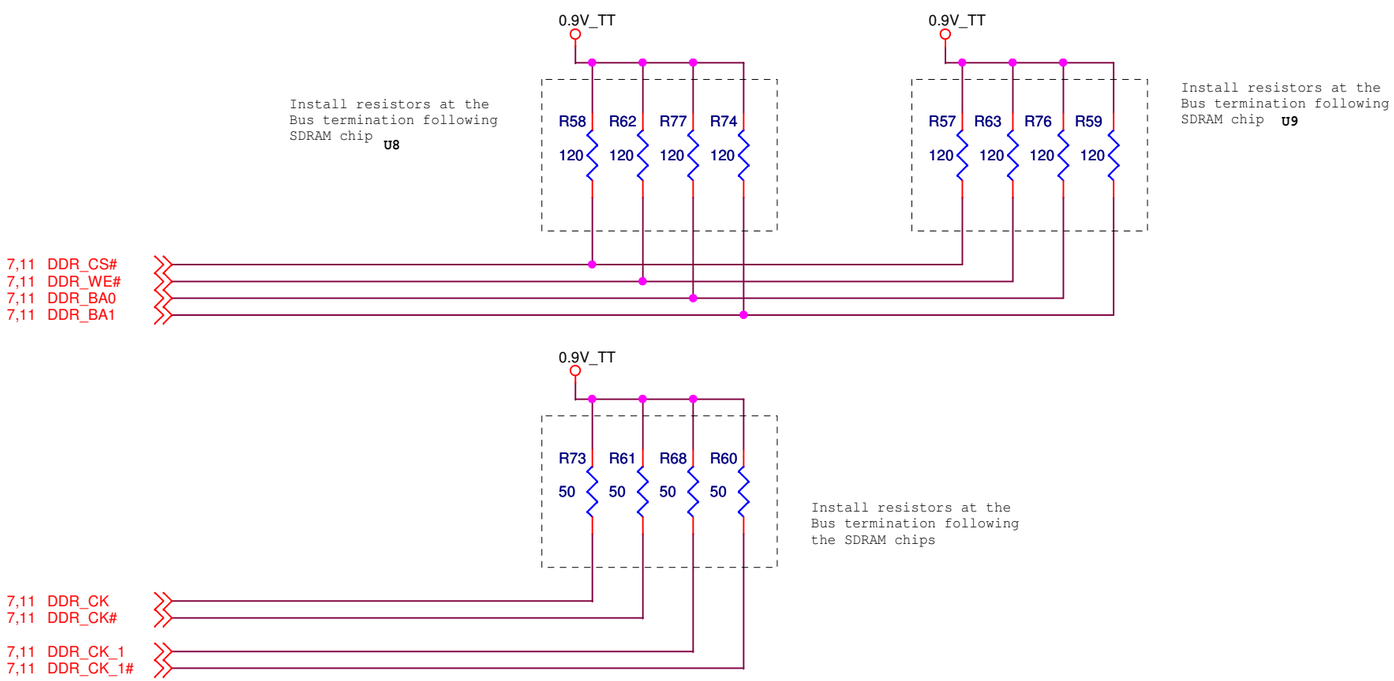
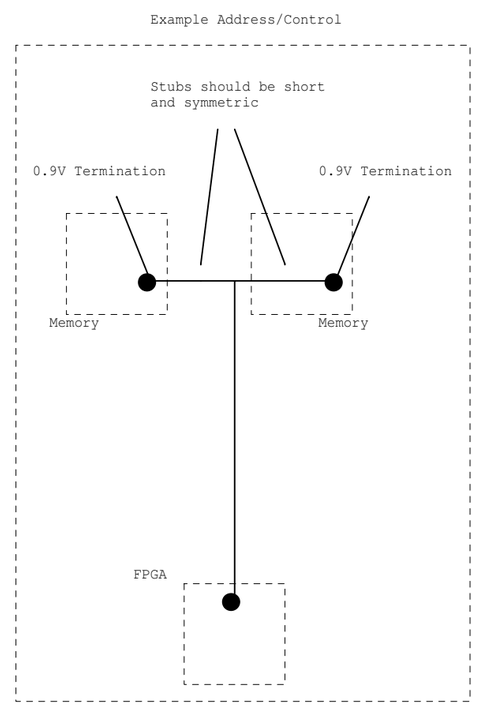
Title	DDR2 SDRAM	
Size C	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Friday, October 06, 2006	Sheet 11 of 24	









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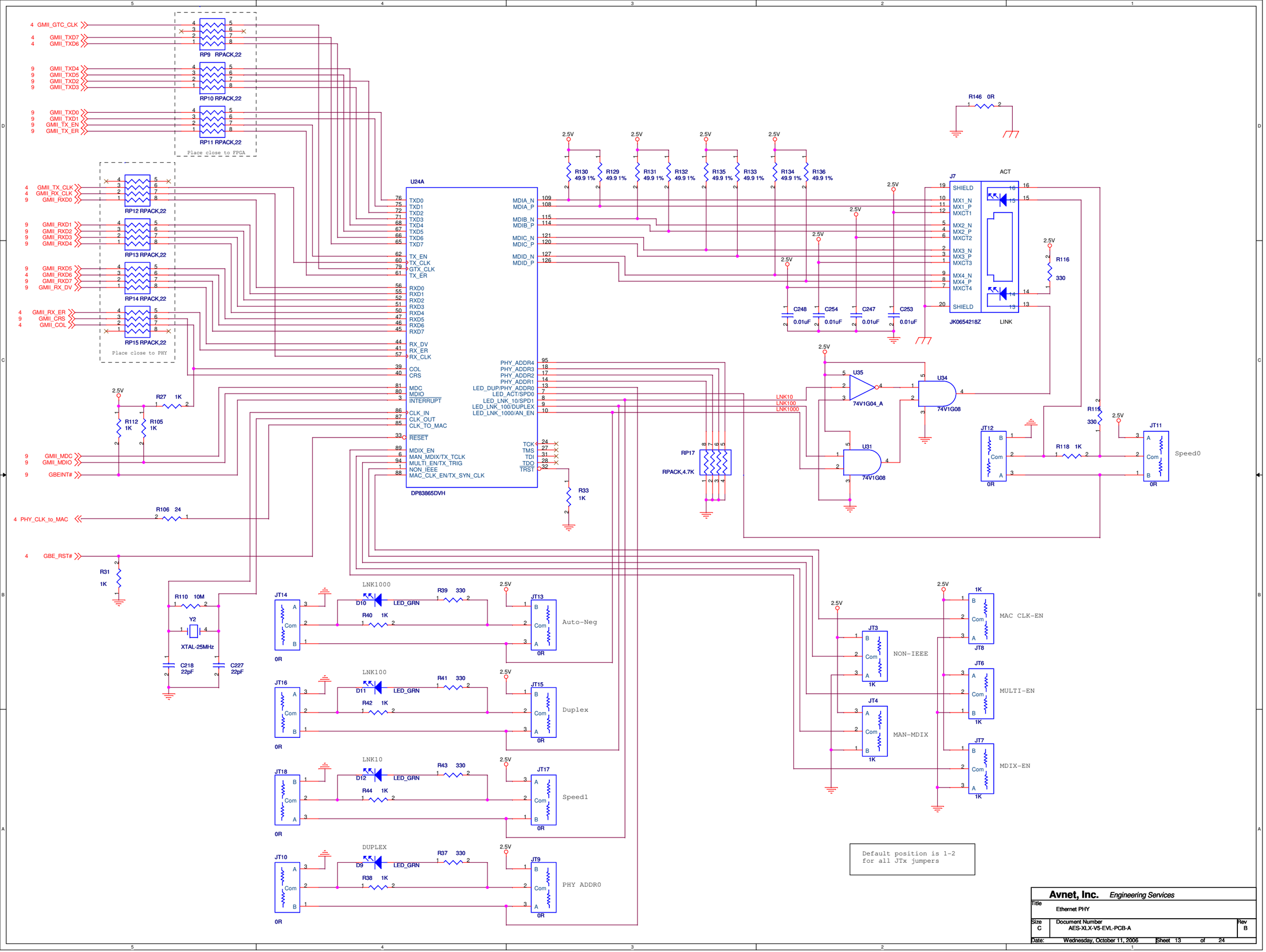
Title	DDR2 Termination	
Size B	Document Number AES-XLX-V5LX-SCH	Rev B
Date: Friday, October 06, 2006	Sheet 12 of 24	


U24A
DP83865DVH
RP9 RPACK,22
RP10 RPACK,22
RP11 RPACK,22
Place close to FPGA
RP12 RPACK,22
RP13 RPACK,22
RP14 RPACK,22
RP15 RPACK,22
Place close to PHY
J7
JK0654218Z
ACT
LINK
U35
74V1G04_A
U34
74V1G08
U31
74V1G08
RP17
RPACK,4.7K
JT12
JT11
Speed0
JT14
JT13
Auto-Neg
JT16
JT15
Duplex
JT18
JT17
Speed1
JT10
JT9
PHY ADDR0
LNK1000
LNK100
LNK10
DUPLEX
JT3
NON-IEEE
JT4
MAN-MDIX
JT8
MAC CLK-EN
JT6
MULTI-EN
JT7
MDIX-EN
Y2
XTAL-25MHz
Default position is 1-2
for all JTx jumpers
Avnet, Inc. Engineering Services
Title
Ethernet PHY
Size C
Document Number
AES-XLX-V5-EVL-PCB-A
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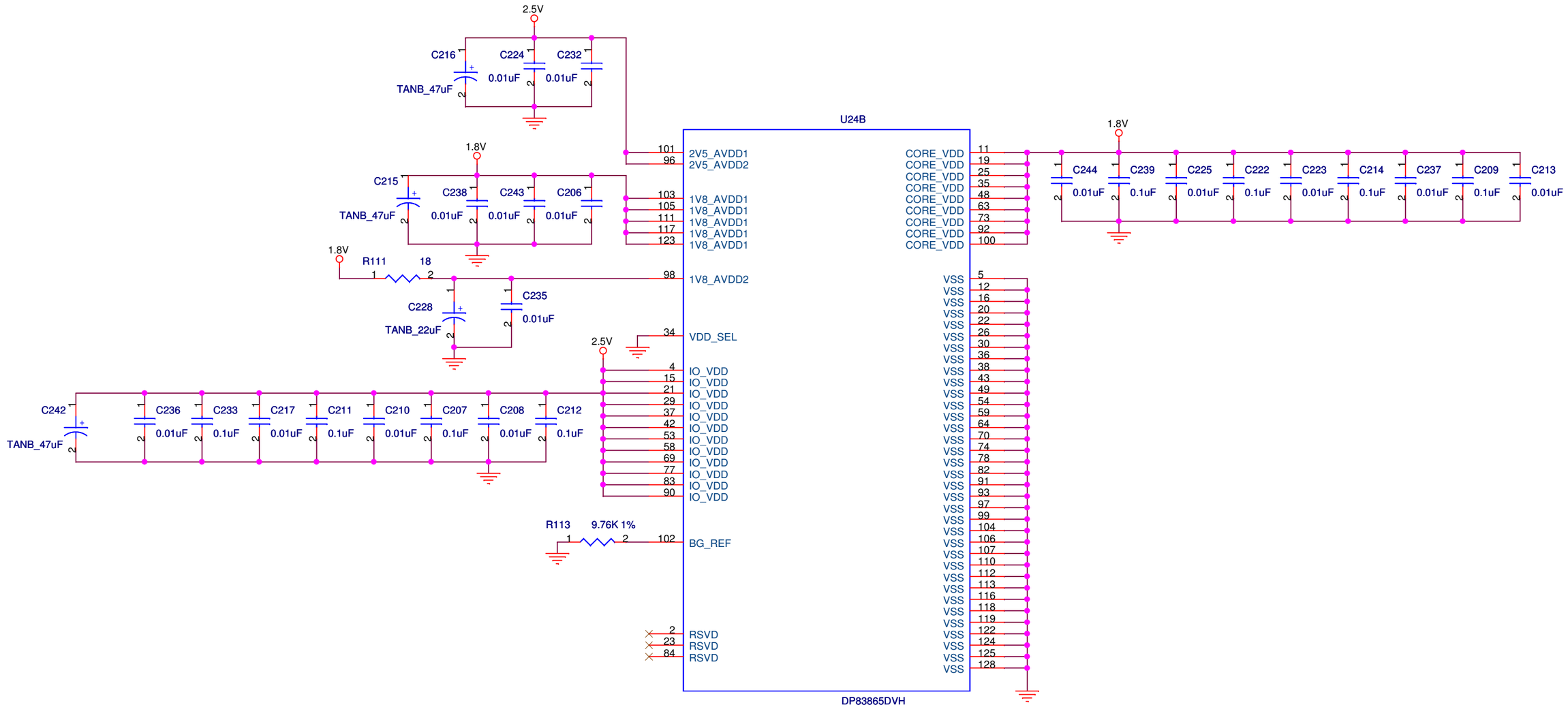

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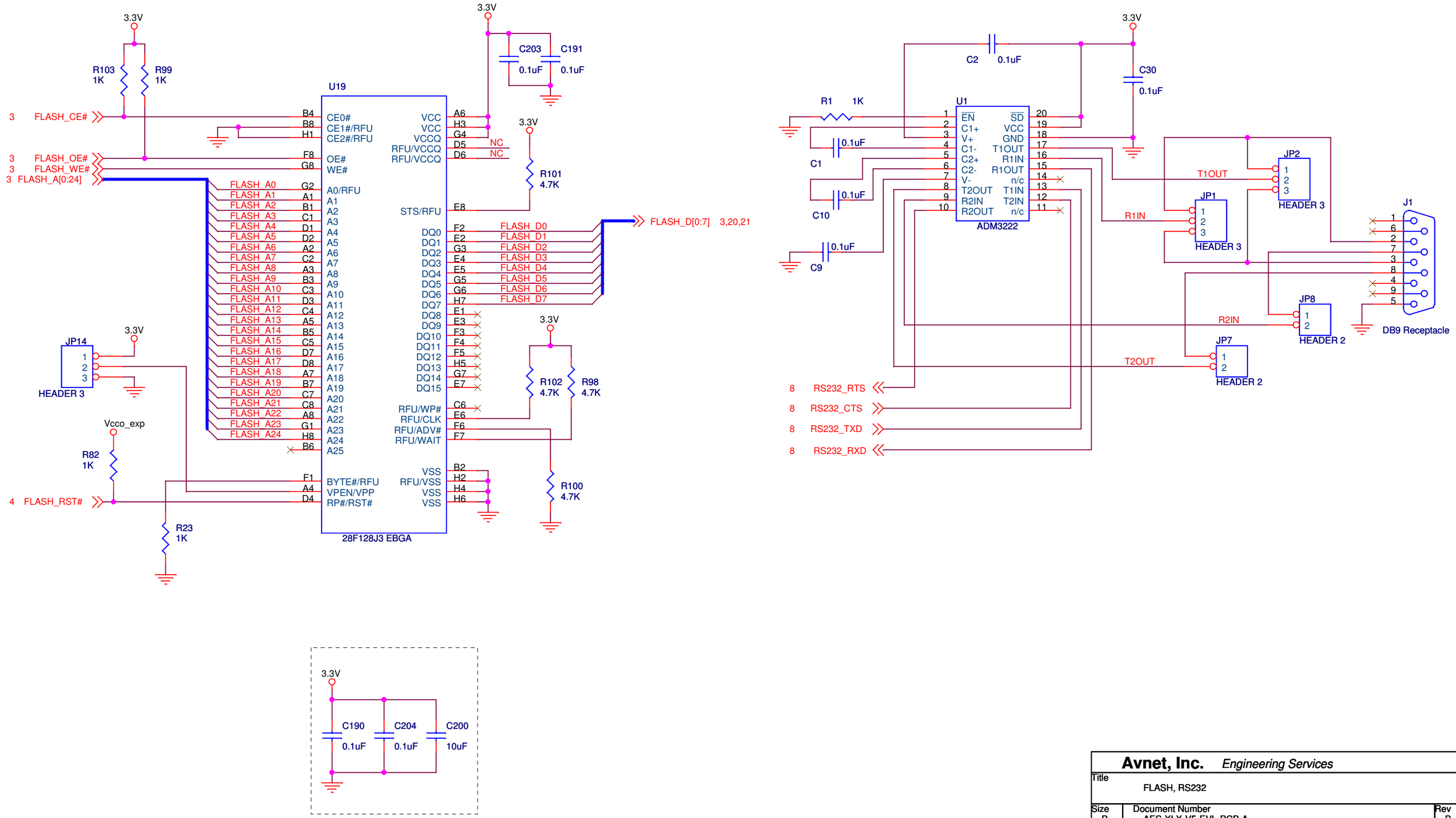
Title: Ethernet Power		
Size: B	Document Number: AES-XLX-V5-EVL-PCB-A	Rev: B
Date: Wednesday, October 04, 2006	Sheet 14 of 24	



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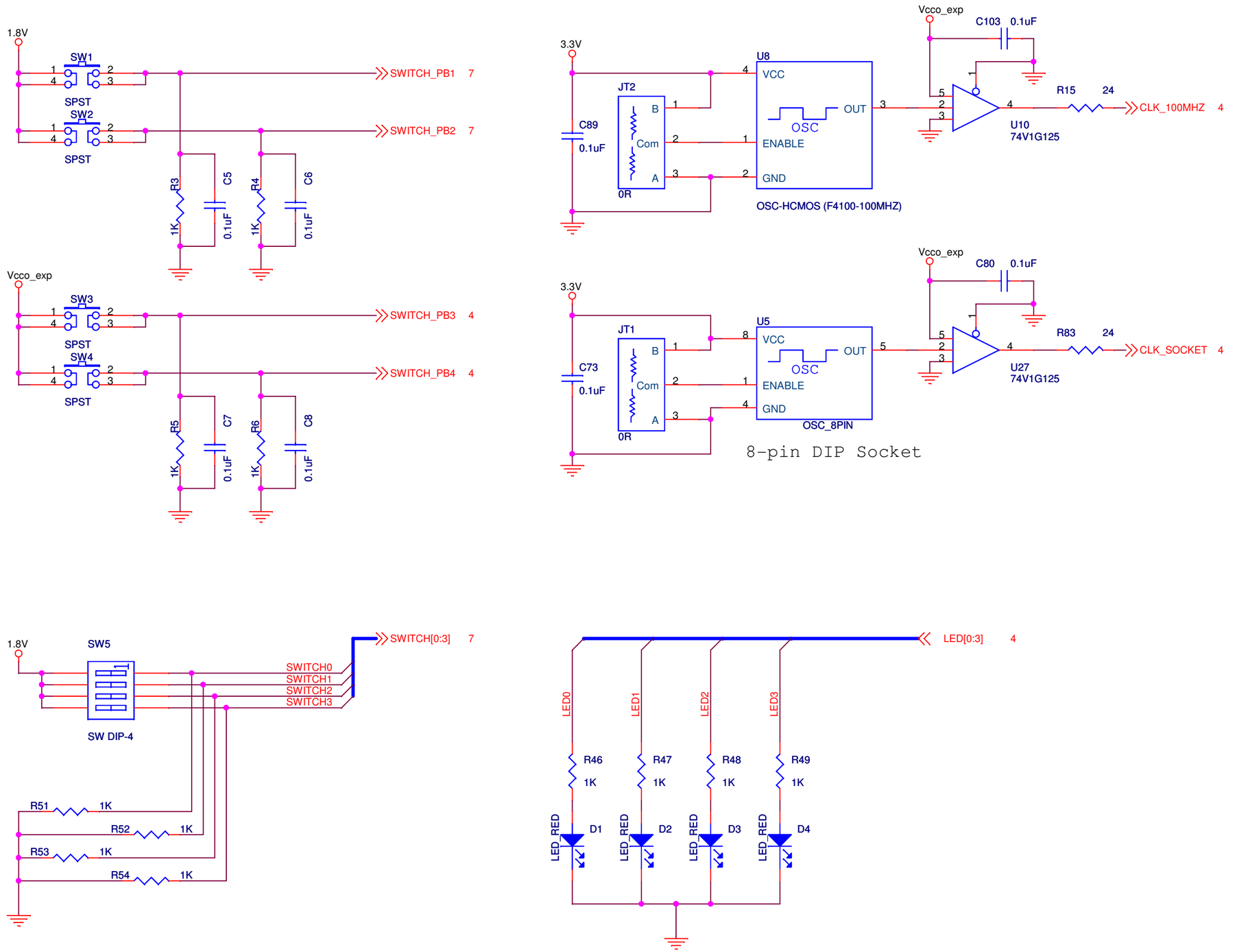
Title	FLASH, RS232	
Size B	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Friday, October 06, 2006	Sheet 15 of 24	



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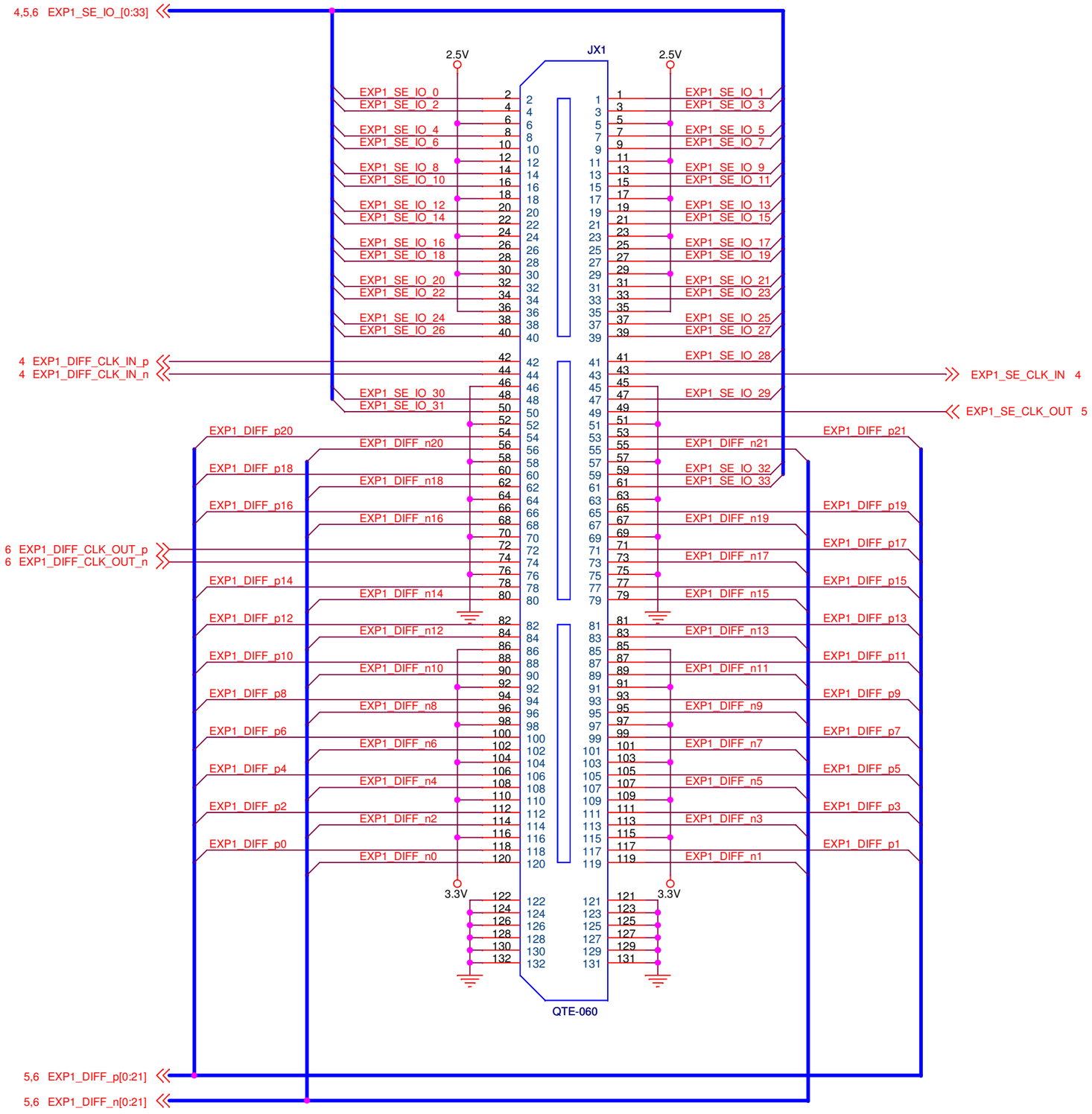
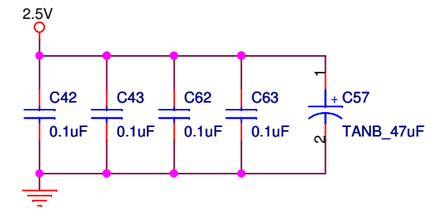
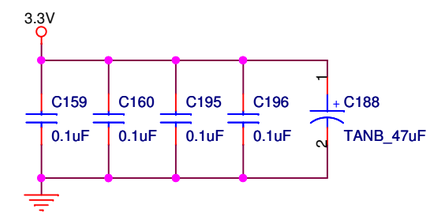
Title: LEDs, Switches, Clocks		
Size: B	Document Number: AES-XLX-V5-EVL-PCB-A	Rev: B
Date: Friday, October 06, 2006	Sheet 16 of 24	







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Title: EXP Connector 1		
Size: B	Document Number: AES-XLX-V5-EVL-PCB-A	Rev: B
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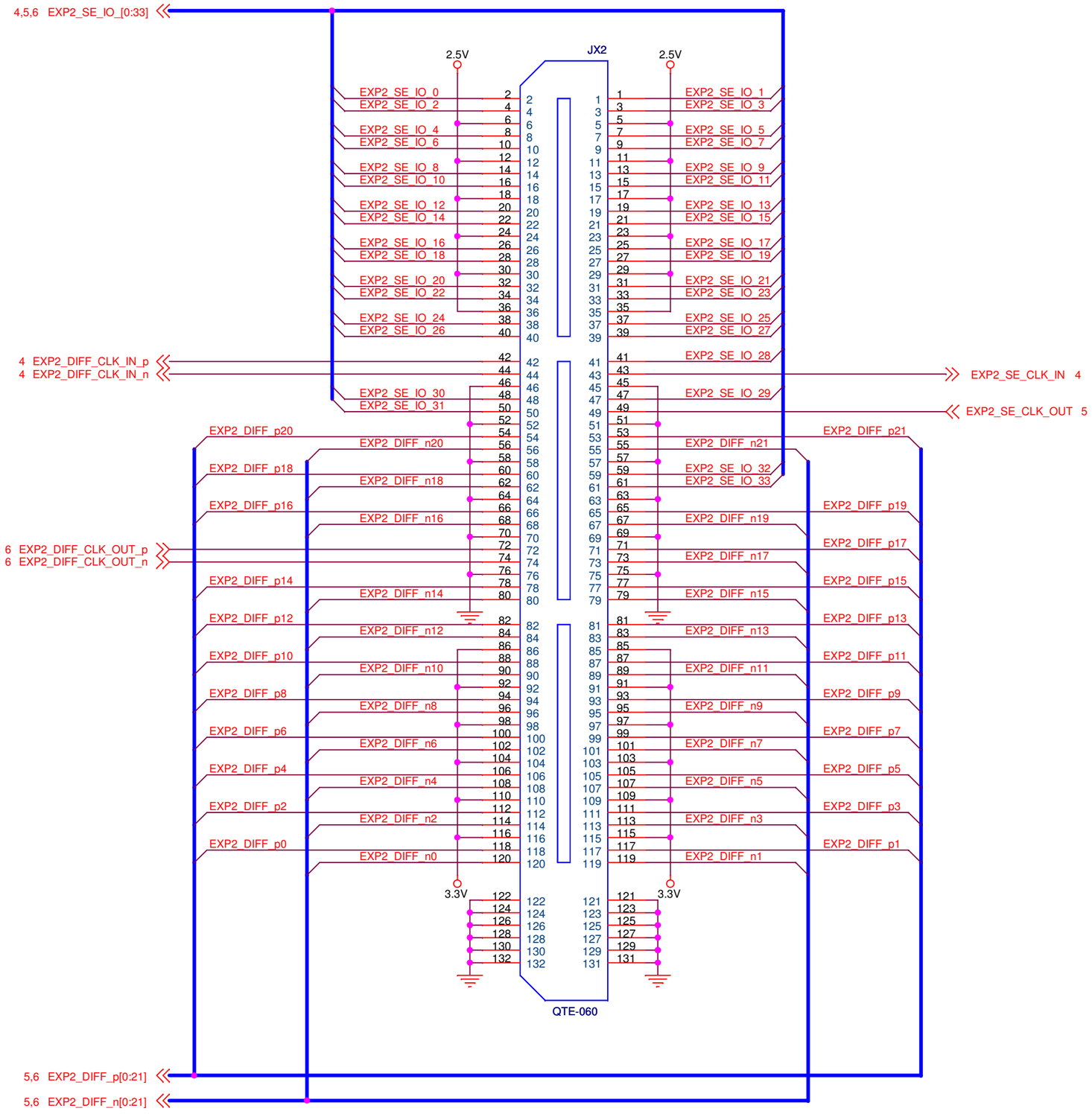

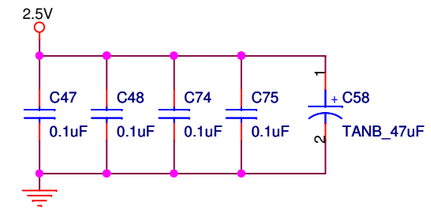

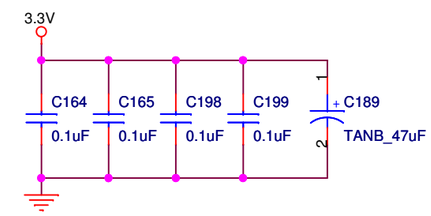

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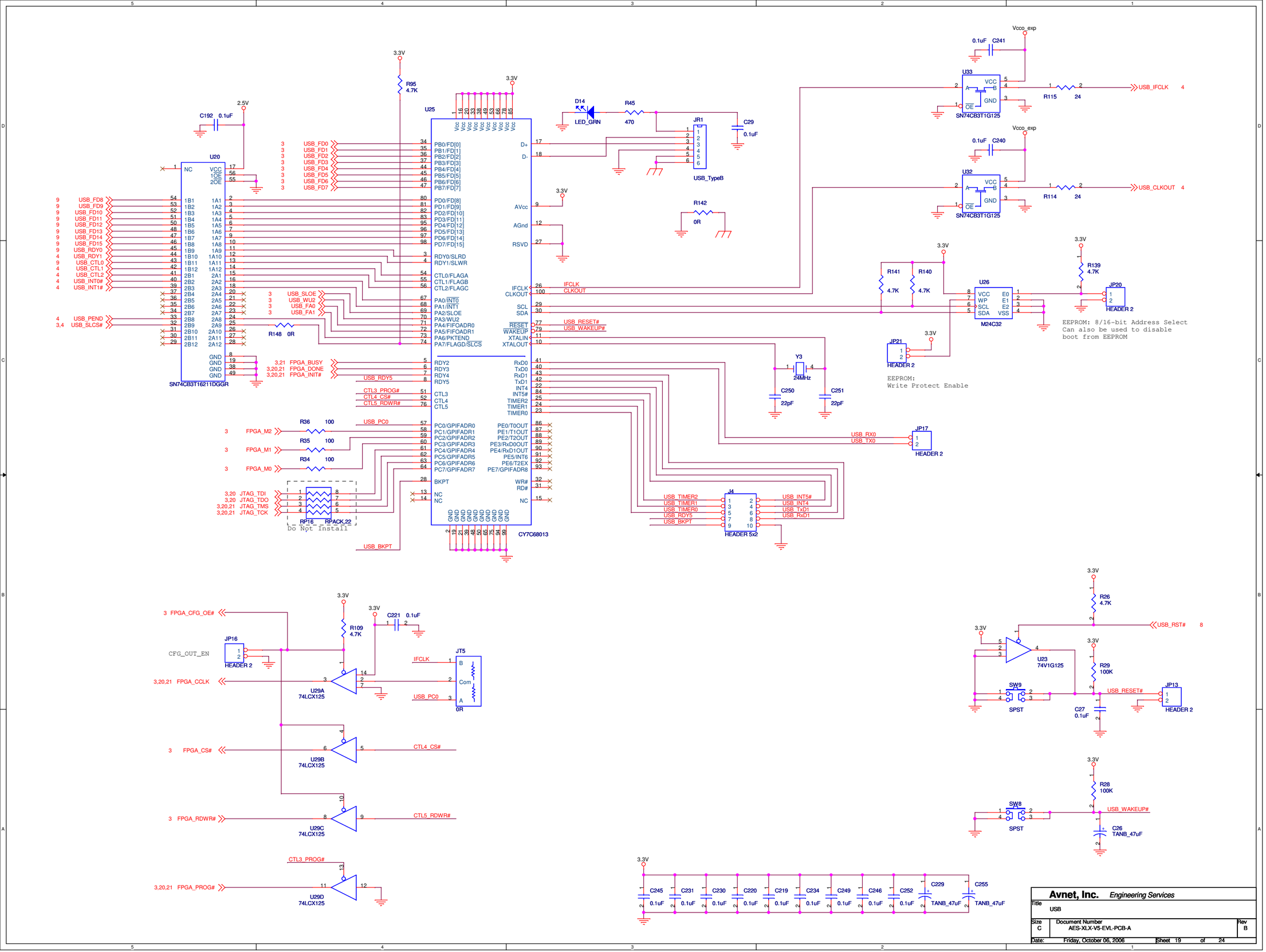
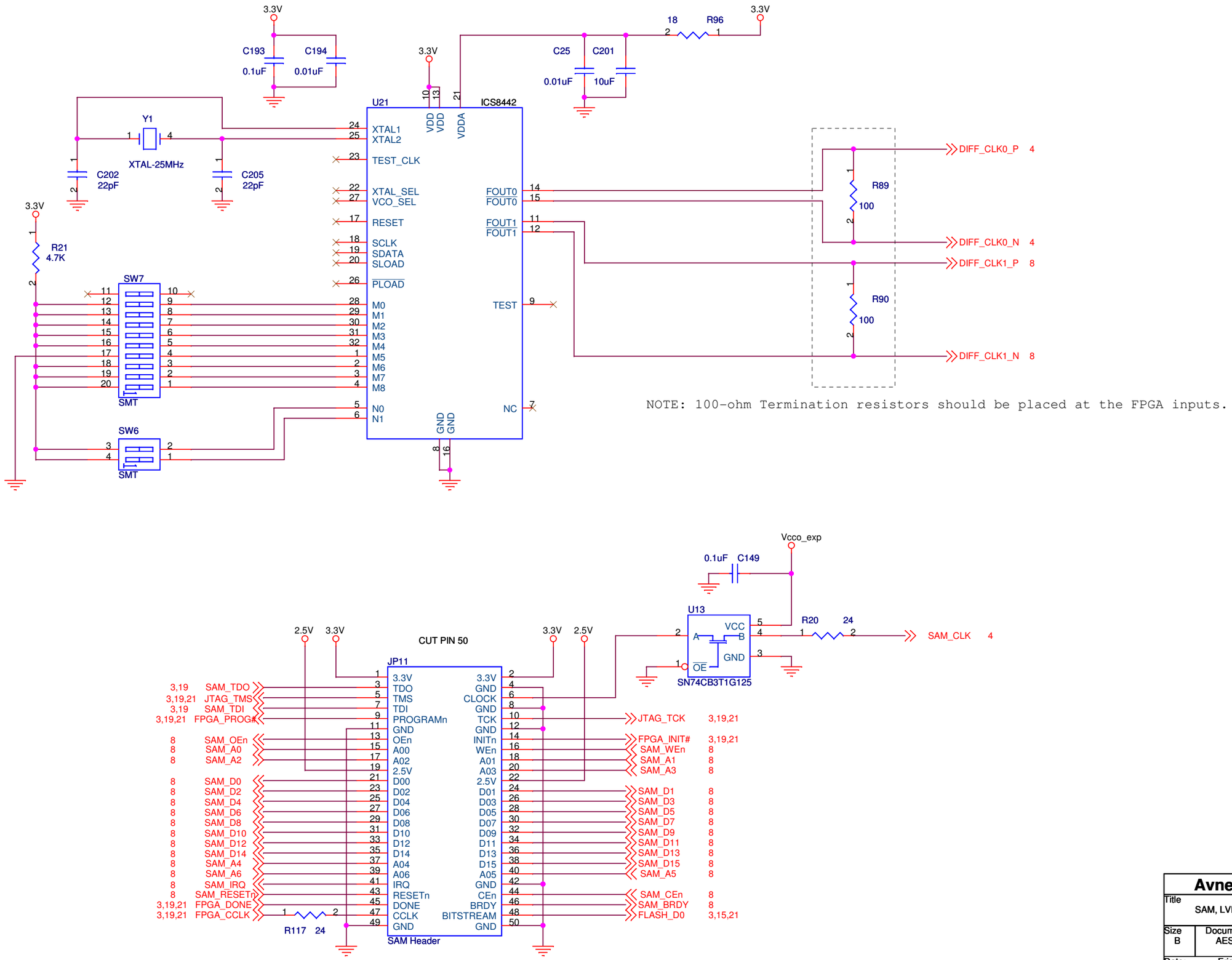
Title	EXP Connector 2	
Size B	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Friday, October 06, 2006	Sheet 18 of 24	

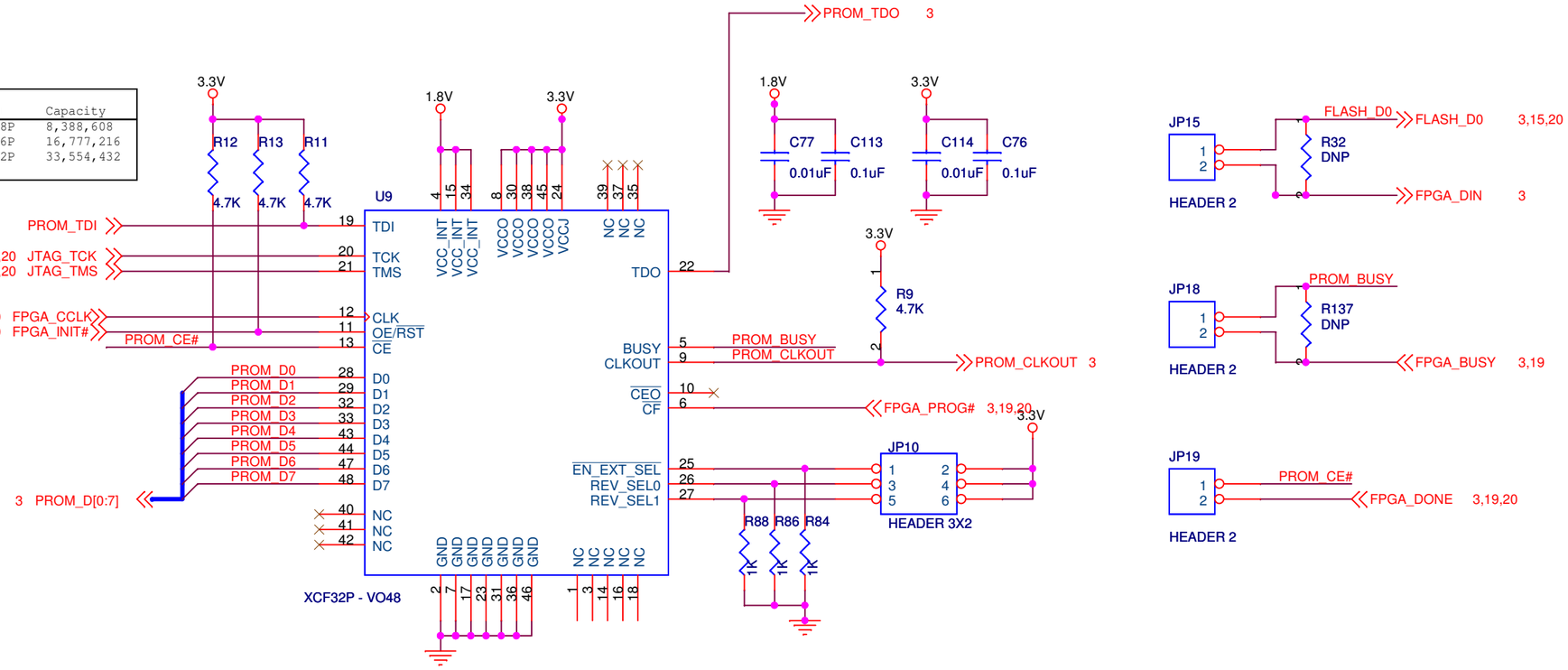

U20
SN74CB3T16211DGGR
U25
CY7C68013
U33
SN74CB3T1G125
U32
SN74CB3T1G125
U26
M24C32
JR1
USB_TypeB
D14
LED_GRN
R45
470
C29
0.1uF
R142
0R
R95
4.7K
C192
0.1uF
C241
0.1uF
C240
0.1uF
R115
24
R114
24
USB_IFCLK
USB_CLKOUT
R141
4.7K
R140
4.7K
R139
4.7K
JP20
HEADER 2
EEPROM: 8/16-bit Address Select
Can also be used to disable
boot from EEPROM
JP21
HEADER 2
EEPROM:
Write Protect Enable
Y3
24MHz
C250
22pF
C251
22pF
JP17
HEADER 2
USB_RX0
USB_TX0
J4
HEADER 5x2
USB_TIMER2
USB_TIMER1
USB_TIMER0
USB_RDY5
USB_BKPT
USB_INT5#
USB_INT4
USB_TxD1
USB_RxD1
R36 100
R35 100
R34 100
FPGA_M2
FPGA_M1
FPGA_M0
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
RP16 RPACK_22
Do Not Install
R148 0R
FPGA_BUSY
FPGA_DONE
FPGA_INIT#
USB_PC0
CTL3_PROG#
CTL4_CS#
CTL5_RDWR#
IFCLK
CLKOUT
USB_RESET#
USB_WAKEUP#
FPGA_CFG_OE#
JP16
HEADER 2
CFG_OUT_EN
R109
4.7K
C221
0.1uF
JT5
0R
FPGA_CCLK
U29A
74LCX125
FPGA_CS#
U29B
74LCX125
FPGA_RDWR#
U29C
74LCX125
FPGA_PROG#
U29D
74LCX125
R26
4.7K
U23
74V1G125
USB_RST#
R29
100K
SW9
SPST
C27
0.1uF
JP13
HEADER 2
R28
100K
SW8
SPST
C26
TANB_47uF
C245
C231
C230
C220
C219
C234
C249
C246
C252
C229
C255
0.1uF
TANB_47uF
Avnet, Inc. Engineering Services
Title USB
Size C
Document Number AES-XLX-V5-EVL-PCB-A
Rev B
Date: Friday, October 06, 2006
Sheet 19 of 24



Avnet, Inc. *Engineering Services*

Title	SAM, LVDS Clock	
Size B	Document Number AES-XLX-V5-EVL-PCB-A	Rev B
Date: Friday, October 06, 2006	Sheet 20 of 24	

PROM	Capacity
XCF08P	8,388,608
XCF16P	16,777,216
XCF32P	33,554,432

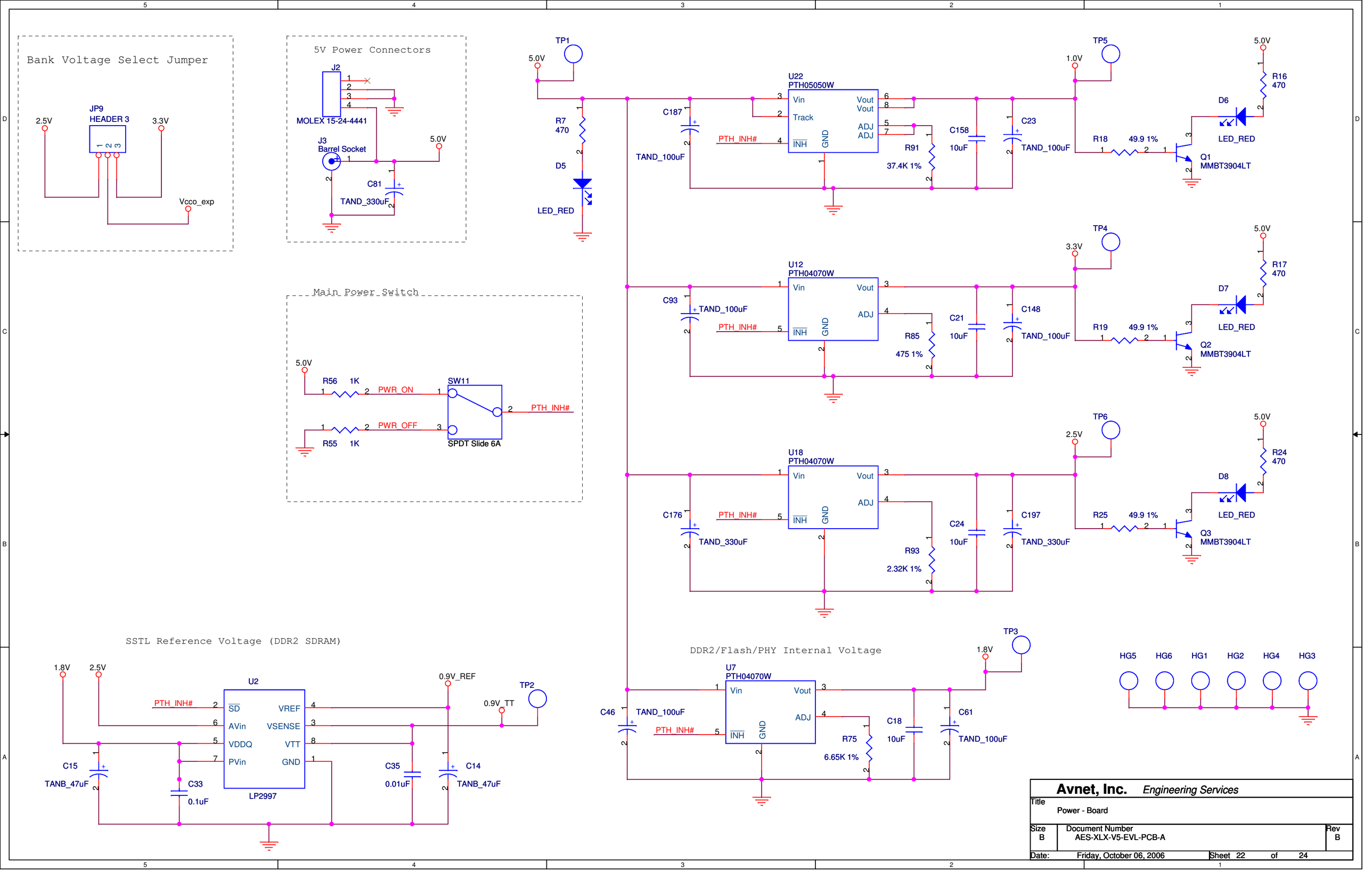


Avnet, Inc. *Engineering Services*

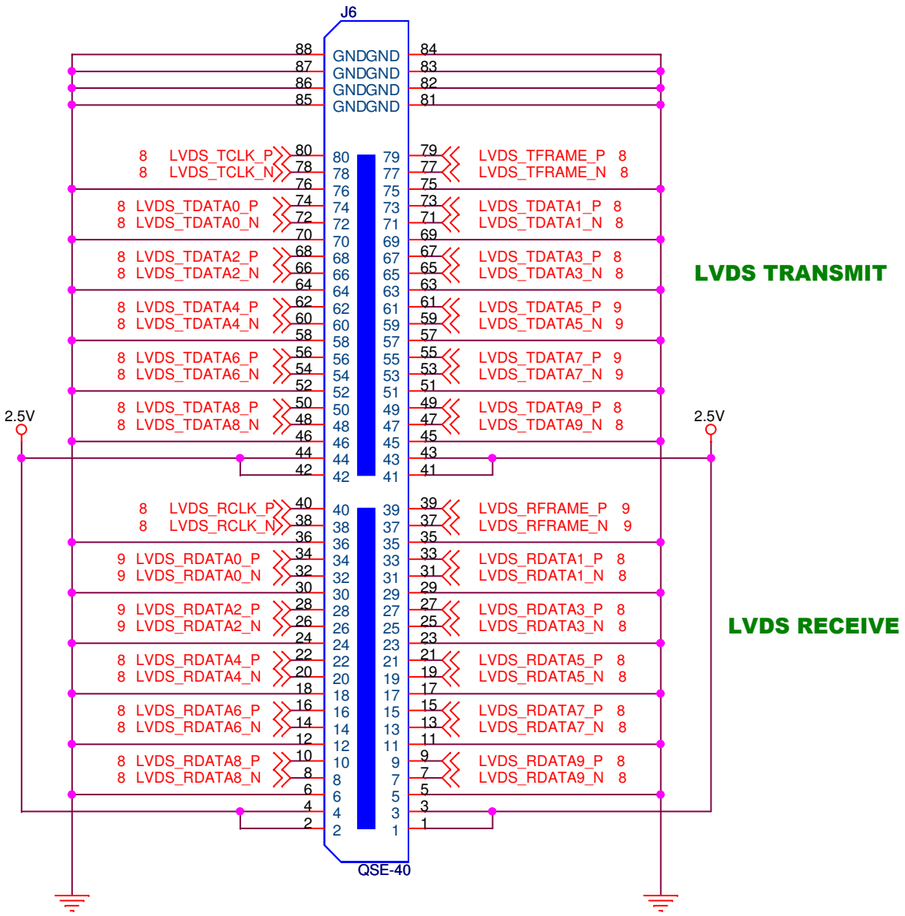
Title: Configuration PROM

Size: B | Document Number: AES-XLX-V5-EVL-PCB-A | Rev: B

Date: Friday, October 06, 2006 | Sheet 21 of 24



Avnet, Inc. *Engineering Services*		
Title: Power - Board		
Size: B	Document Number: AES-XLX-V5-EVL-PCB-A	Rev: B
Date: Friday, October 06, 2006	Sheet 22 of 24	

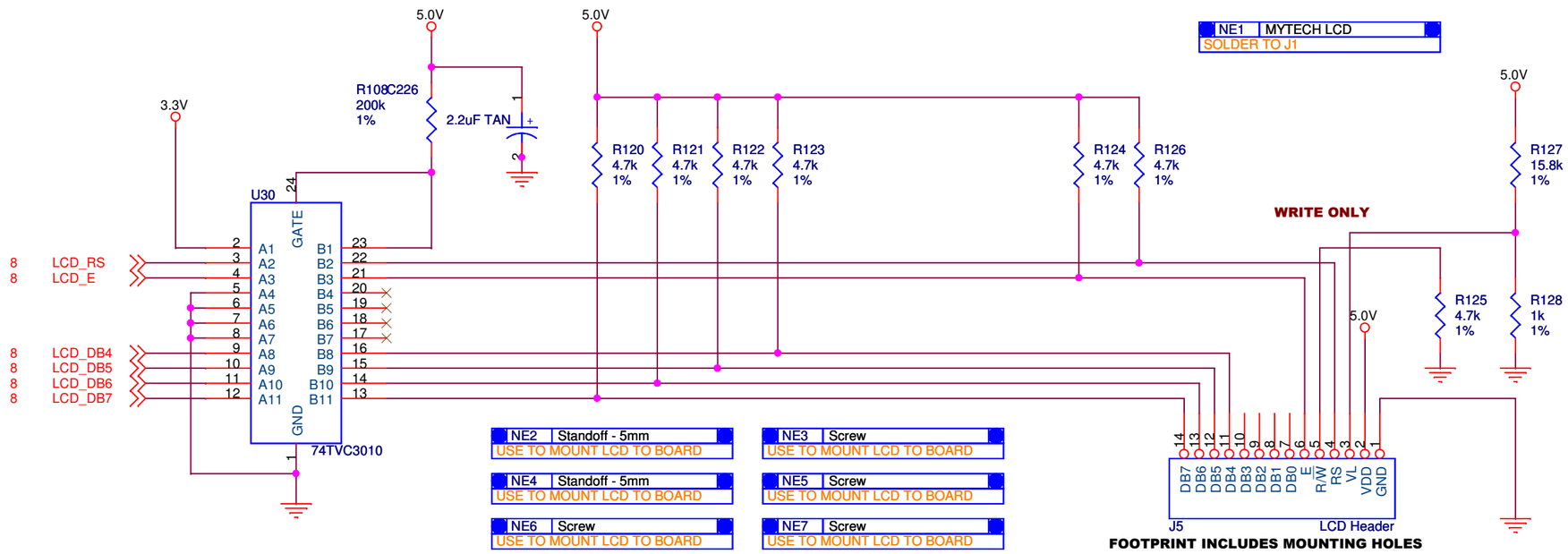


LVDS TRANSMIT

LVDS RECEIVE

Avnet, Inc. *Engineering Services*		
Title: LVDS Connectors		
Size: B	Document Number: AES-XLX-V5LX-SCH	Rev: B
Date: Friday, October 06, 2006	Sheet 23 of 24	

LCD MODULE CONNECTOR



** LCD display wired to run in 4 bit mode

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Title	LCD	
Size B	Document Number AES-XLX-V5LX-SCH	Rev B
Date: Friday, October 06, 2006	Sheet 24 of 24	