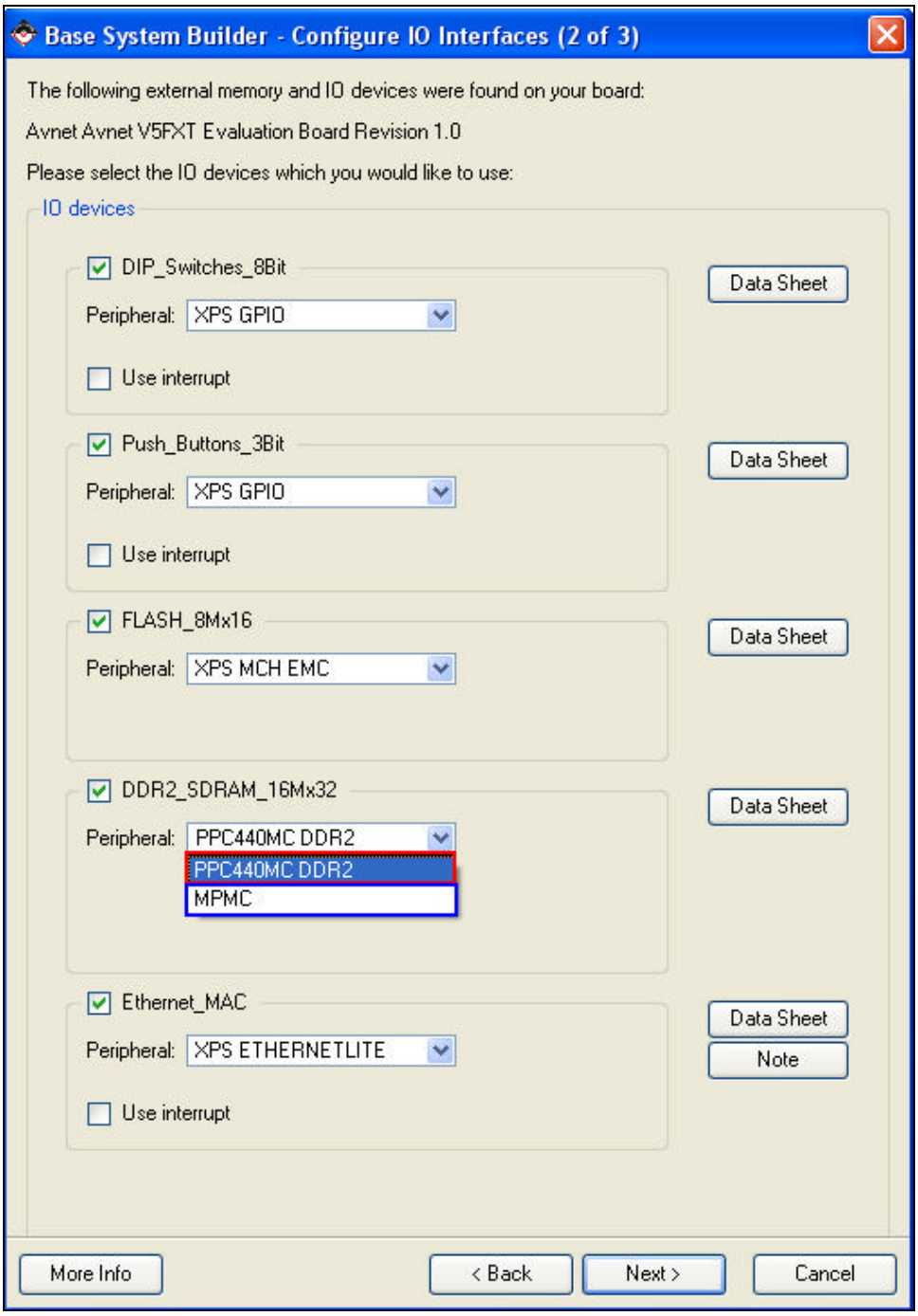
Avnet V5FXT Evaluation Board BSB Errata

In a PowerPC 440 based system, the EDK 10.1.02 Base System Builder (BSB) allows the user to connect the on-board DDR2 memory to the processor via the **PPC440MC DDR2** controller (default option) or the **MPMC** core as shown in the following BSB screen shot for the Avnet V5FXT evaluation board.



When the **PPC440MC DDR2** controller is used to interface to the on-board DDR2 memory on the Avnet V5FXT evaluation board, BSB generates the following PPC440 processor parameters (shown in the box) incorrectly (there are no issues with using the MPMC core). These parameters must be modified in order for the PPC440 interface to the DDR2 memory on the Avnet V5FXT evaluation board to work properly.

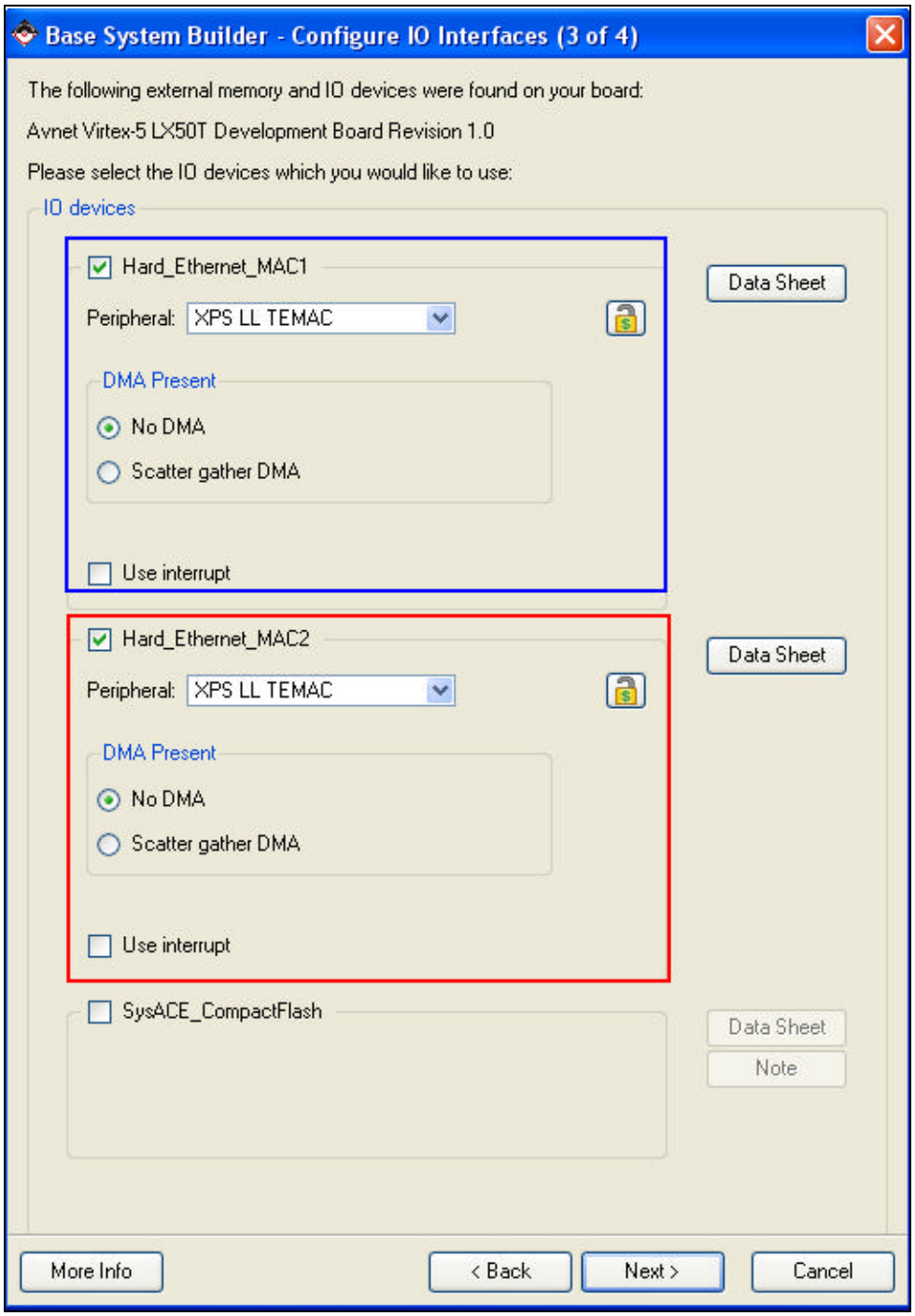
```
74  BEGIN ppc440_virtex5
75   PARAMETER INSTANCE = ppc440_0
76   PARAMETER HW_VER = 1.01.a
77   PARAMETER C_PPC440MC_ROW_CONFLICT_MASK = 0x003FFE00
78   PARAMETER C_PPC440MC_BANK_CONFLICT_MASK = 0x00C00000
79   PARAMETER C_PPC440MC_CONTROL = 0xf810008f
80   PARAMETER C_IDCR_BASEADDR = 0b0000000000
81   PARAMETER C_IDCR_HIGHADDR = 0b0011111111
82   BUS_INTERFACE MPLB = plb_v46_0
83   BUS_INTERFACE PPC440MC = ppc440_0_PPC440MC
84   BUS_INTERFACE JTAGPPC = jtagppc_cntlr_0_0
85   BUS_INTERFACE RESETPPC = ppc_reset_bus
86   PORT CPMC440CLK = proc_clk_s
87   PORT CPMPPCMPLBCLK = sys_clk_s
88   PORT CPMPPCSOPLBCLK = sys_clk_s
89   PORT CPMINTERCONNECTCLKNTO1 = net_vcc
90   PORT CPMMCCLK = sys_clk_s
91   PORT CPMINTERCONNECTCLK = proc_clk_s
92  END
```

After creating the design using BSB, please open the **system.mhs** file in the XPS GUI, modify the PPC440 parameters as shown in the following figure, and save the **system.mhs** file prior to implementing your design.

```
74  BEGIN ppc440_virtex5
75   PARAMETER INSTANCE = ppc440_0
76   PARAMETER HW_VER = 1.01.a
77   PARAMETER C_PPC440MC_ROW_CONFLICT_MASK = 0x000FFF80
78   PARAMETER C_PPC440MC_BANK_CONFLICT_MASK = 0x00300000
79   PARAMETER C_PPC440MC_CONTROL = 0xf850008f
80   PARAMETER C_IDCR_BASEADDR = 0b0000000000
81   PARAMETER C_IDCR_HIGHADDR = 0b0011111111
82   BUS_INTERFACE MPLB = plb_v46_0
83   BUS_INTERFACE PPC440MC = ppc440_0_PPC440MC
84   BUS_INTERFACE JTAGPPC = jtagppc_cntlr_0_0
85   BUS_INTERFACE RESETPPC = ppc_reset_bus
86   PORT CPMC440CLK = proc_clk_s
87   PORT CPMPPCMPLBCLK = sys_clk_s
88   PORT CPMPPCSOPLBCLK = sys_clk_s
89   PORT CPMINTERCONNECTCLKNTO1 = net_vcc
90   PORT CPMMCCLK = sys_clk_s
91   PORT CPMINTERCONNECTCLK = proc_clk_s
92  END
```

Avnet V5LXT/SXT PCIe Development Board BSB Errata

The Avnet V5LXT/SXT PCIe development board (V5LX50T, V5LX110T, V5SX50T, and V5SX95T versions) provides two on-board 10/100/1000 PHY devices. In the EDK 10.1.02 BSB, user has the option of using a soft Ethernet MAC (default option) or the Virtex-5 integrated hard TEMAC core to connect to the on-board 10/100/1000 PHY devices as shown in the following BSB screen shot for the Avnet V5LX50T development board.



If both hard TEMAC cores are used in a design (as shown in the above BSB screen shot), BSB fails to include the following TEMAC ports (shown in the box in the following figure) for the second TEMAC instantiated in the design.

After creating the design using BSB, please open the **system.mhs** file in the XPS GUI, modify the second instance of the TEMAC core to add the missing ports as shown in the following figure, and save the **system.mhs** file prior to implementing your design.

```
303  BEGIN xps_ll_temac
304   PARAMETER INSTANCE = Hard_Ethernet_MAC2
305   PARAMETER HW_VER = 1.01.b
306   PARAMETER C_SPLB_CLK_PERIOD_PS = 7500
307   PARAMETER C_PHY_TYPE = 1
308   PARAMETER C_TEMAC_TYPE = 0
309   PARAMETER C_TEMAC1_ENABLED = 0
310   PARAMETER C_TEMAC0_PHYADDR = 0b00000000000000000000000000000001
311   PARAMETER C_NUM_IDELAYCTRL = 2
312   PARAMETER C_IDELAYCTRL_LOC = IDELAYCTRL_X0Y5-IDELAYCTRL_X1Y1
313   PARAMETER C_BASEADDR = 0x81c20000
314   PARAMETER C_HIGHADDR = 0x81c2ffff
315   BUS_INTERFACE SPLB = mb_plb
316   BUS_INTERFACE LLINK0 = Hard_Ethernet_MAC2llink0
317   PORT TemacPhy_RST_n = fpga_0_Hard_Ethernet_MAC2_TemacPhy_RST_n
318   PORT GMII_TXD_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TXD_0
319   PORT GMII_TX_EN_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TX_EN_0
320   PORT GMII_TX_ER_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TX_ER_0
321   PORT GMII_TX_CLK_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TX_CLK_0
322   PORT GMII_RXD_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RXD_0
323   PORT GMII_RX_DV_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RX_DV_0
324   PORT GMII_RX_ER_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RX_ER_0
325   PORT GMII_RX_CLK_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RX_CLK_0
326   PORT MII_TX_CLK_0 = fpga_0_Hard_Ethernet_MAC2_MII_TX_CLK_0
327   PORT MDC_0 = fpga_0_Hard_Ethernet_MAC2_MDC_0
328   PORT MDIO_0 = fpga_0_Hard_Ethernet_MAC2_MDIO_0
329   PORT GTX_CLK_0 = temac_clk_s
330   PORT REFCLK = clk_200mhz_s
331   PORT LlinkTemac0_CLK = sys_clk_s
332  END
```