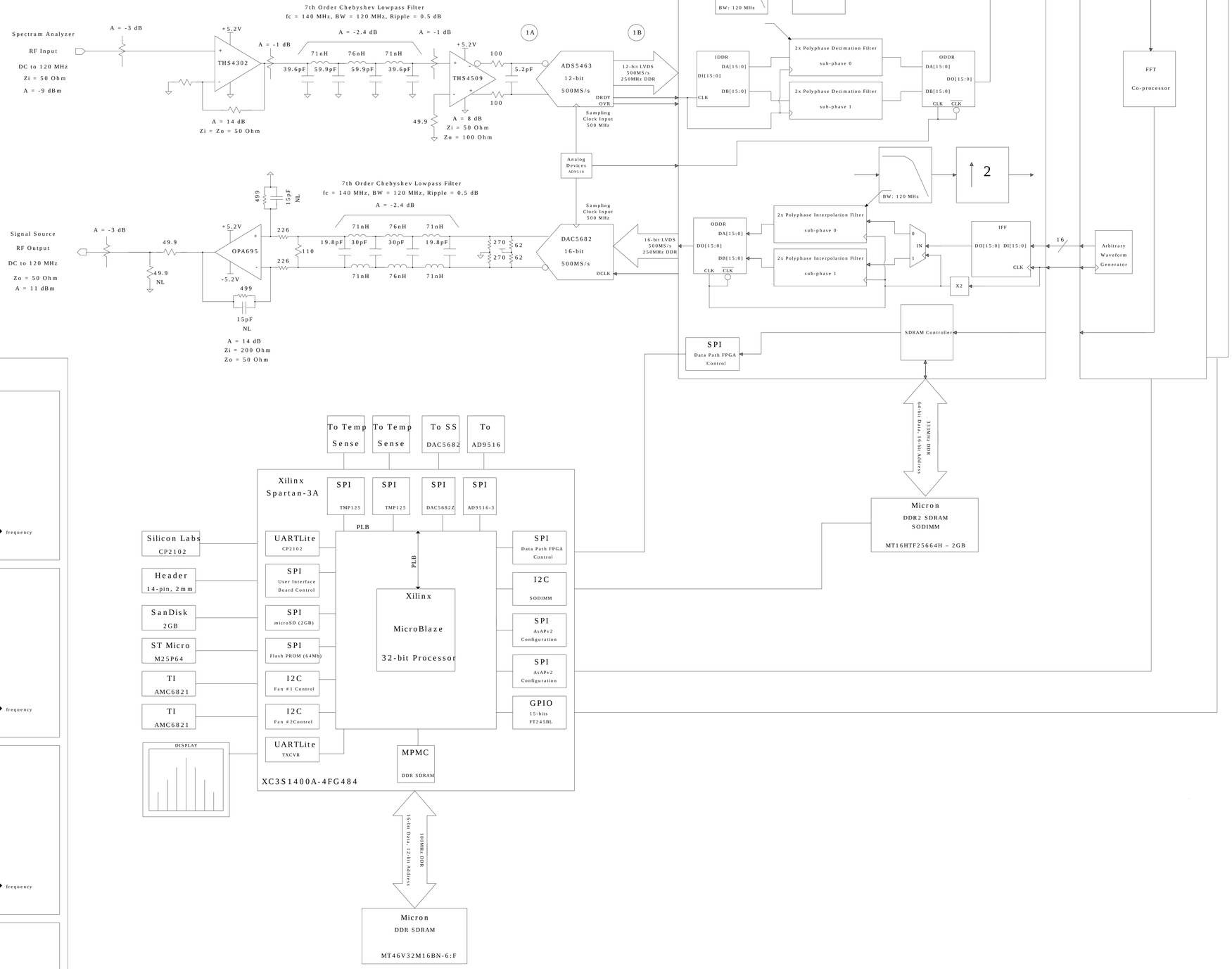
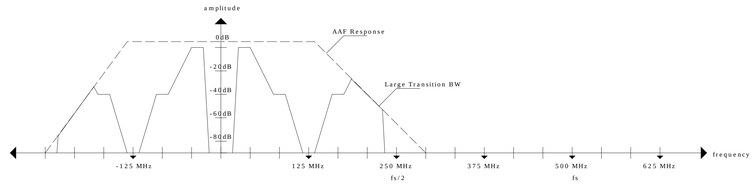
UC Davis ECE MSEE Thesis

Measurement Board Block Diagram

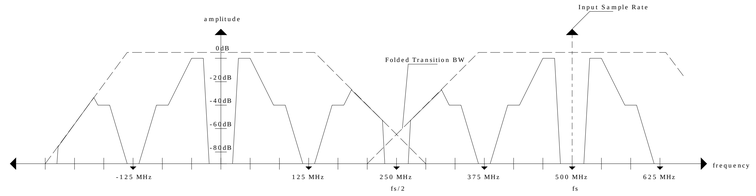


Spectrum Analyzer Spectra Analysis

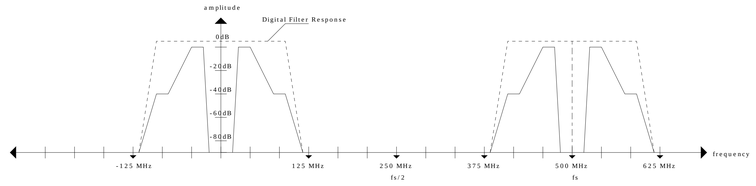
1A Spectrum at Output of Analog Anti-Alias Filter



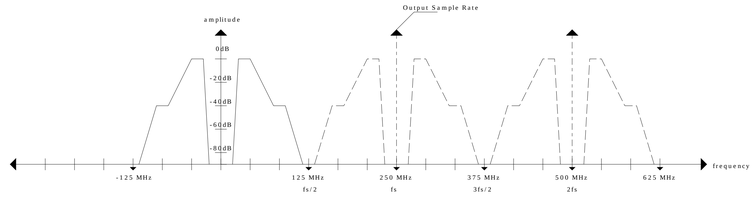
1B Spectrum at Output of ADC



1C Spectrum at Output of Digital Anti-Alias Filter



1D Spectrum at Output of 2-to-1 Down Sampler



VLSI Computation LAB

Title:	BLOCK DIAGRAM		
File:	MEAS_MAIN_BOARD		
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Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 1 of 43	REV: 001

A INDEX

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Title:	SCHEMATIC INDEX		
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Notes and References

Data Sheets and User Guides:

Xilinx Virtex-5 SX50T:

1. Data Sheet: http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
2. DC and Switching: http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf
3. User Guide: http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
4. Packaging and Pinout: http://www.xilinx.com/support/documentation/user_guides/ug195.pdf
5. Configuration Guide: http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
6. Rocket I/O GTP Guide: http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
7. PCB Designer's Guide: http://www.xilinx.com/support/documentation/user_guides/ug203.pdf
8. System Monitor Guide: http://www.xilinx.com/support/documentation/user_guides/ug192.pdf

Xilinx Spartan-3A XC3S1400A:

1. Data Sheet: http://www.xilinx.com/support/documentation/data_sheets/ds529.pdf
2. User Guide: http://www.xilinx.com/support/documentation/user_guides/ug331.pdf
3. Configuration Guide: http://www.xilinx.com/support/documentation/user_guides/ug332.pdf

Samsung QDR-II SRAM:

1. K7R323684C-EC250 Data Sheet: http://www.samsung.com/global/system/business/semiconductor/product/2007/7/30/948789ds_k7r32xx84c_rev11.pdf

TI ADS5463 12-bit, 500MS/s:

1. ADS5463 Data Sheet: http://focus.ti.com/lit/ds/symlink/ads5463.pdf

TI DAC5682Z 16-bit, 1GS/s:

1. DAC5682Z Data Sheet: http://focus.ti.com/lit/ds/symlink/dac5682z.pdf

TI High-Speed Op-Amps: THS4302, THS4509, OPA695

1. THS4302 Data Sheet: http://focus.ti.com/lit/ds/symlink/ths4302.pdf
2. THS4509 Data Sheet: http://focus.ti.com/lit/ds/symlink/ths4509.pdf
3. OPA695 Data Sheet: http://focus.ti.com/lit/ds/symlink/opa695.pdf

TI Power Supply Regulators:

1. PTH08T220WAZ Data Sheet: http://focus.ti.com/lit/ds/symlink/pth08t220w.pdf
2. PTH08T260WAZ Data Sheet: http://focus.ti.com/lit/ds/symlink/pth08t260w.pdf
3. PTH12050YAZ Data Sheet: http://focus.ti.com/lit/ds/symlink/pth12050y.pdf
4. TPS79601 Data Sheet: http://focus.ti.com/lit/ds/symlink/tps79601.pdf
5. TPS74201 Data Sheet: http://focus.ti.com/lit/ds/symlink/tps74201.pdf
6. TPS73701 Data Sheet: http://focus.ti.com/lit/ds/symlink/tps73701.pdf
7. LP2951D Data Sheet: http://focus.ti.com/lit/ds/symlink/lp2951.pdf
8. TPS72301 Data Sheet: http://focus.ti.com/lit/ds/symlink/tps72301.pdf
9. TL7733BCD Data Sheet: http://focus.ti.com/lit/ds/symlink/tl7733b.pdf
10. TPS3808G25 Data Sheet: http://focus.ti.com/lit/ds/symlink/tps3808g25.pdf

TI Fan Controllers

1. AMC6821 Data Sheet: http://focus.ti.com/lit/ds/symlink/amc6821.pdf

Micron DDR2 SDRAM SODIMM:

1. MT16HTF25664HY-667E1 Data Sheet: http://download.micron.com/pdf/datasheets/modules/ddr2/HTF16C128 256x64H.pdf

Analog Devices Clock PLL IC:

1. AD9516-3 Data Sheet: http://www.analog.com/UploadedFiles/Data_Sheets/AD9516_3.pdf

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Title:	NOTES AND REFERENCES		
File:	MEAS_MAIN_BOARD		
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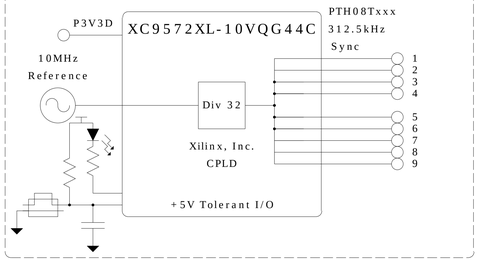
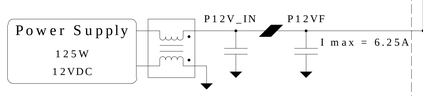
PCB NO: 342	Size: E	Sheet 4 of 43	REV: 001

Power Generation Block Diagram

*** PTH08Txxx Sync Gen ***

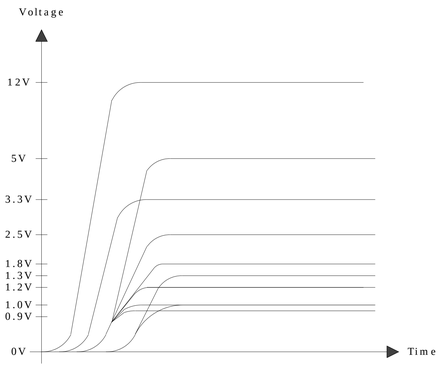


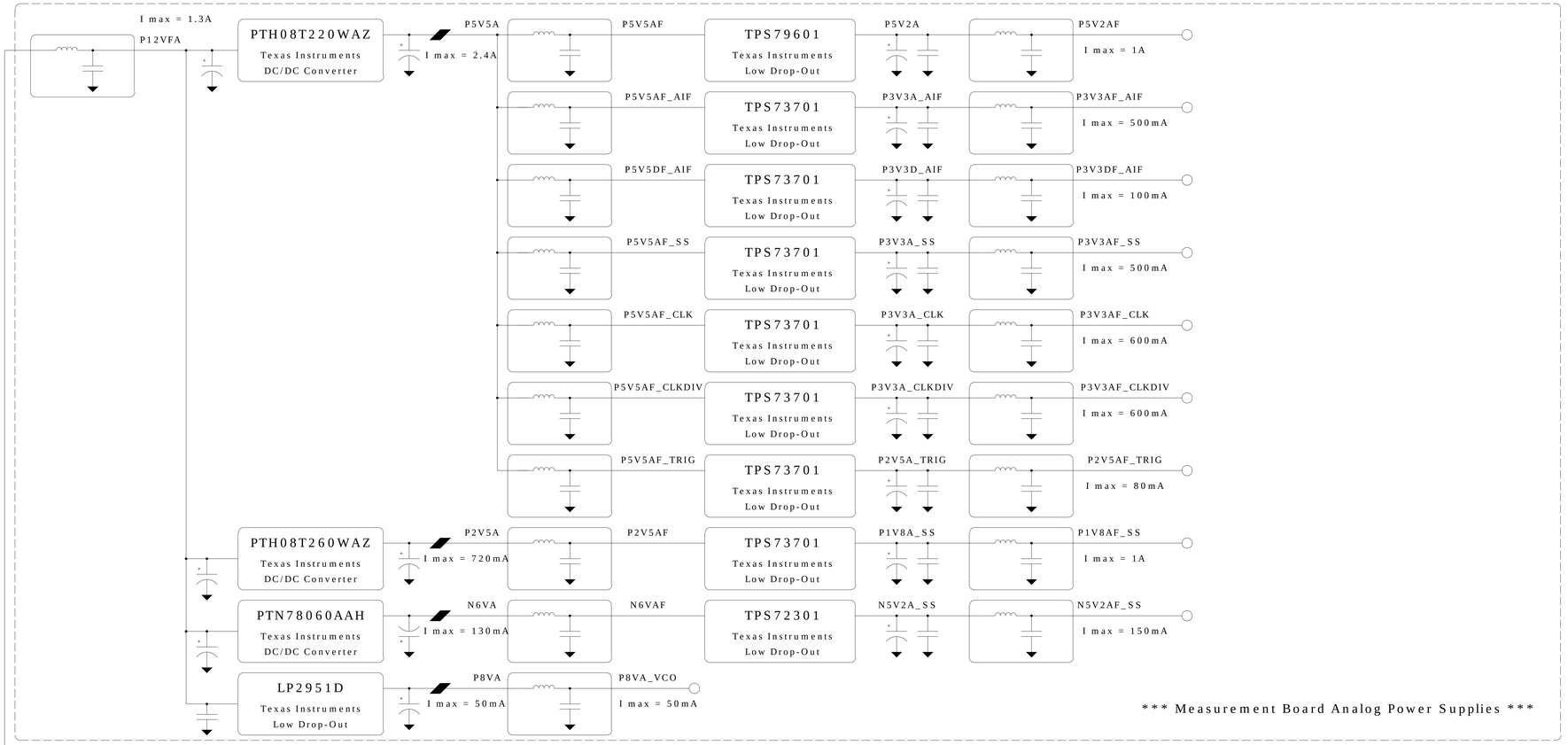
*** Input Supply Conditioning ***



Total Power Usage: 75W

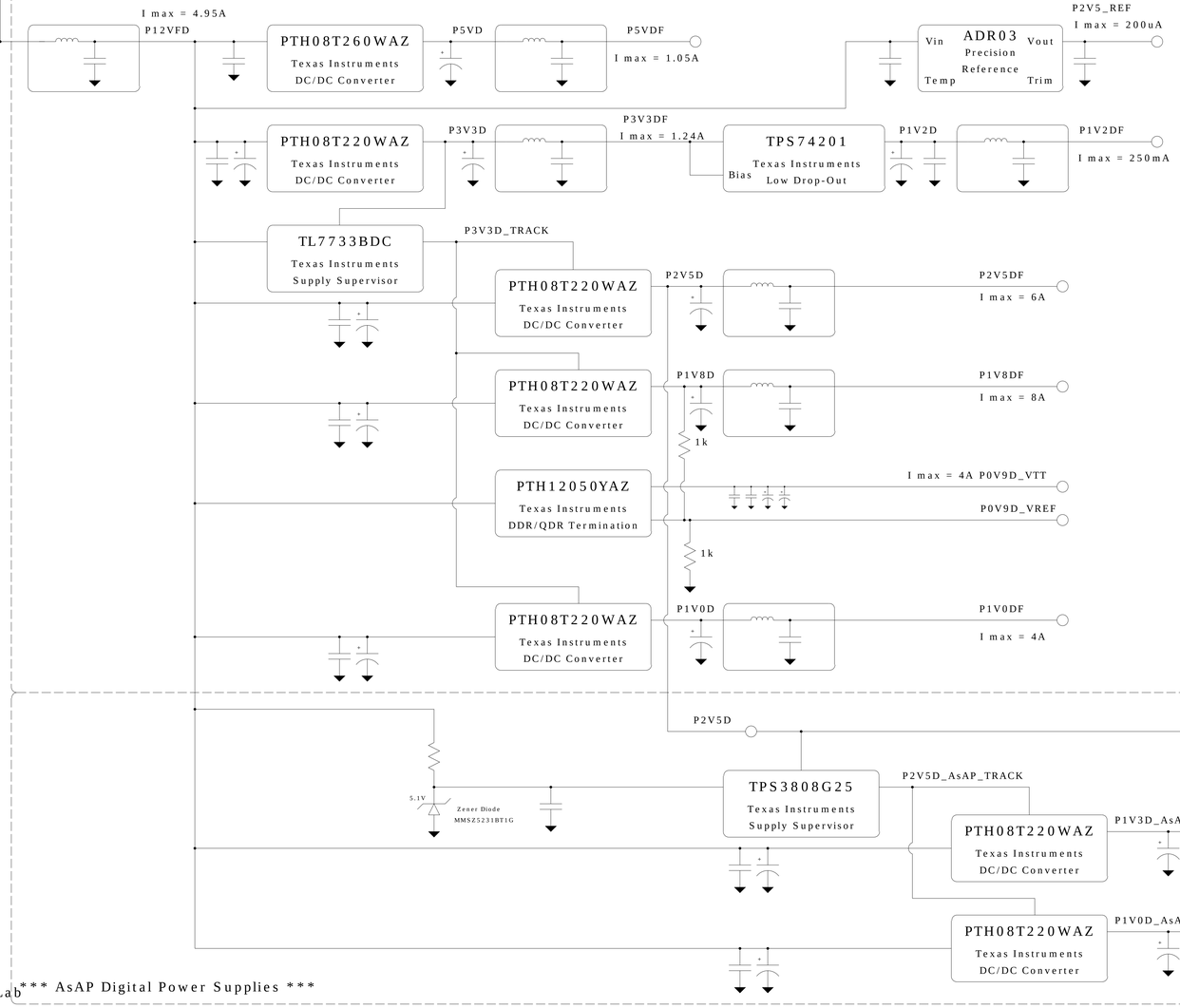
Digital Power Supply Sequencing





*** Measurement Board Analog Power Supplies ***

*** Measurement Board Digital Power Supplies ***



*** AsAP Digital Power Supplies ***

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File:	MEAS_MAIN_BOARD		
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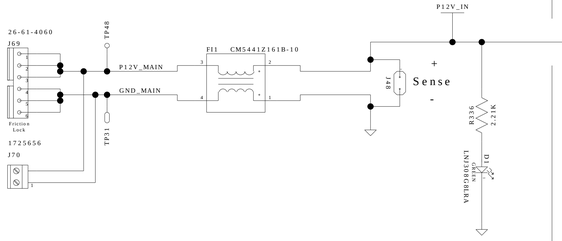
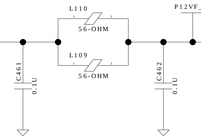
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 5 of 43	REV: 001

MAIN POWER INPUT AND FAN CONTROL

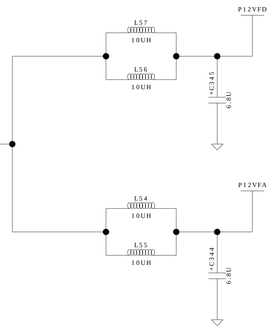
A +12V SUPPLY INPUT



B +12V Filtering

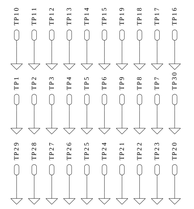


C +12V Analog and Digital Filtering

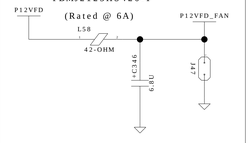


D GROUND Tst Pts

Spread out over board - Top & Bottom

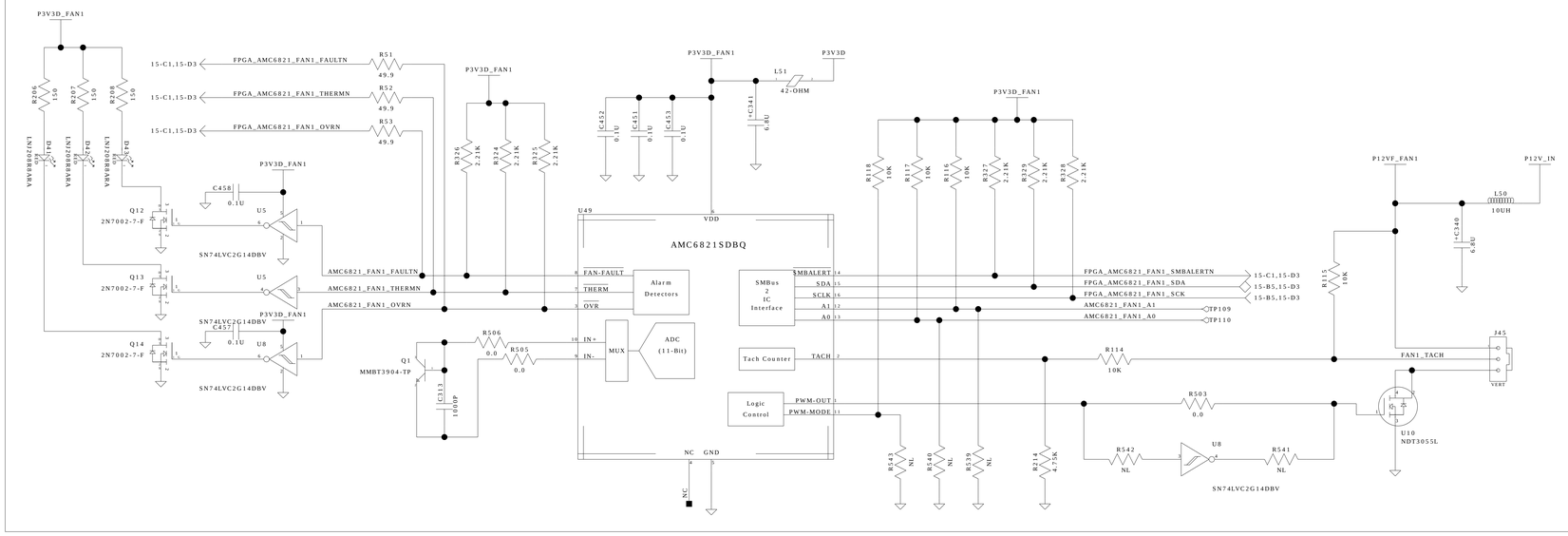


E FPGA Fan

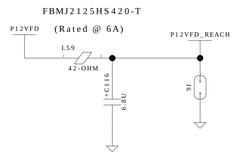


Place on perimeter of FPGA.

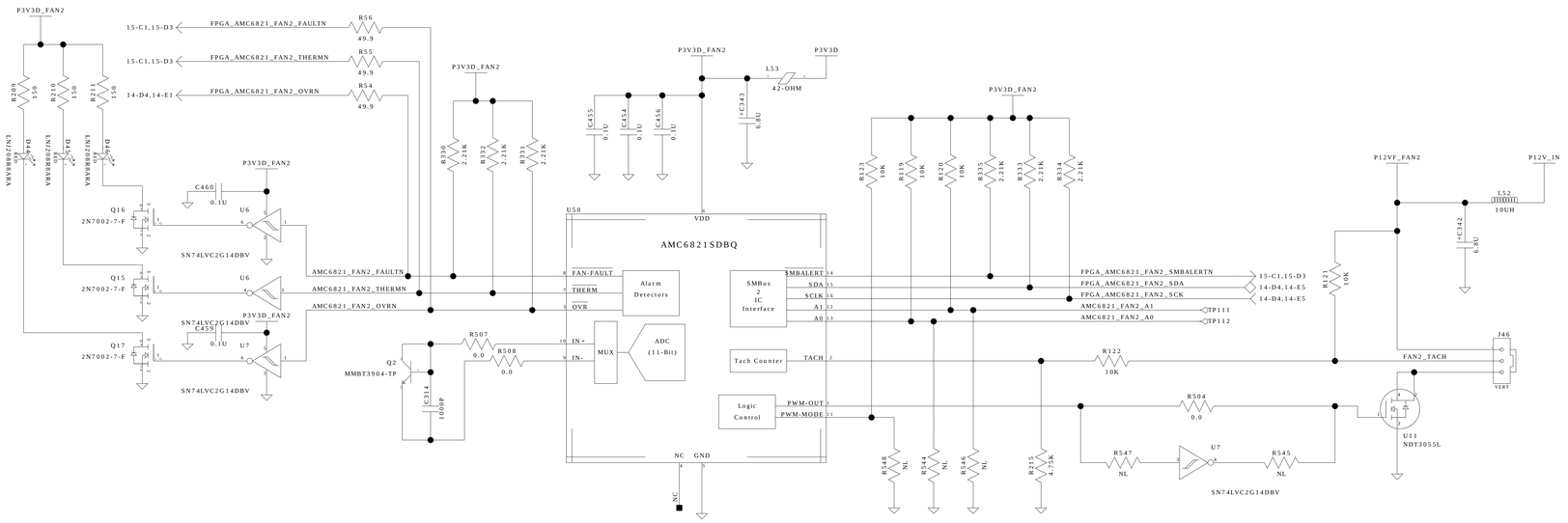
F Instrument Fan #1 Control



G Reach Display PWR



H Instrument Fan #2 Control



VLSI Computation LAB

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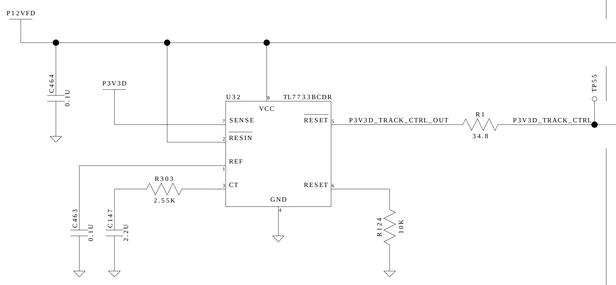
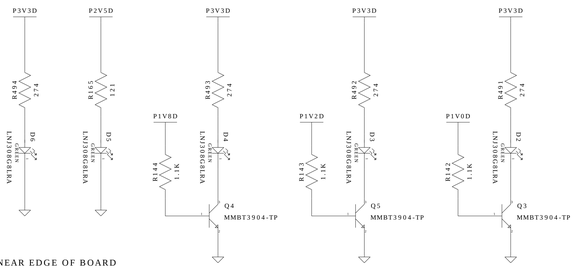
Xilinx Virtex-5 SX50T Digital Supply Regulation and Sequencing

A Digital Supply Sequencers



B POWER LEDs



PLACE LEDs NEAR EDGE OF BOARD

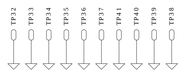
Green LED (LNJ308G8LRA):

RLED = (VCC - VF)/IF

VF = 1.9V IF = 5mA

C GROUND Tst Pts

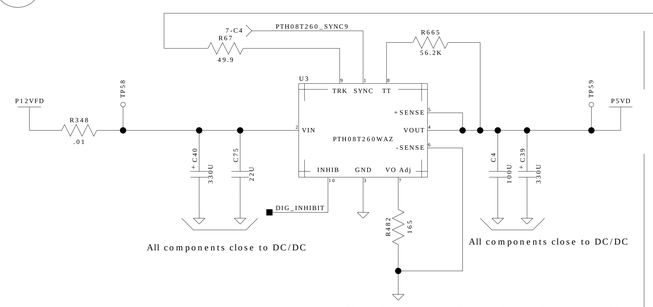
Spread out over board - Top & Bottom



D PTH08T220WAZ DISABLE

Load Jumper to Disable DC/DC Converters

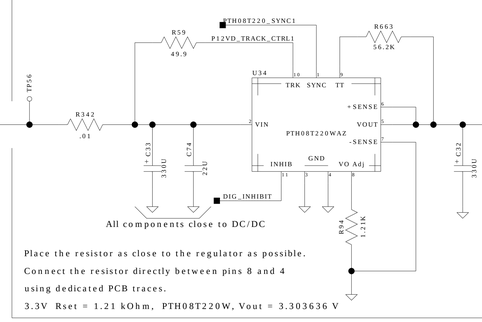
E +5V Digital Supply Regulation



5.0V Rset = 165 Ohm, PTH08T260W, Vout = 5.01 V

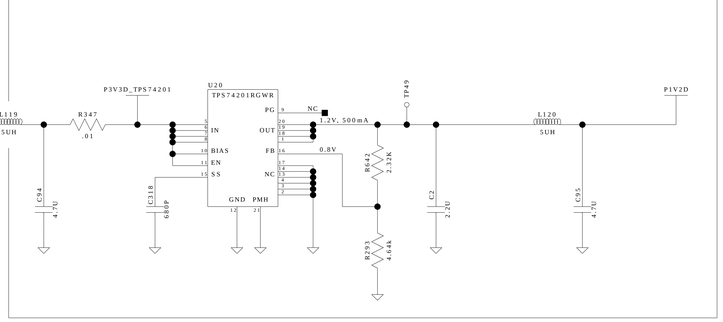
Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 7 and 3
using dedicated PCB traces.

F +3.3V Digital Power Supply

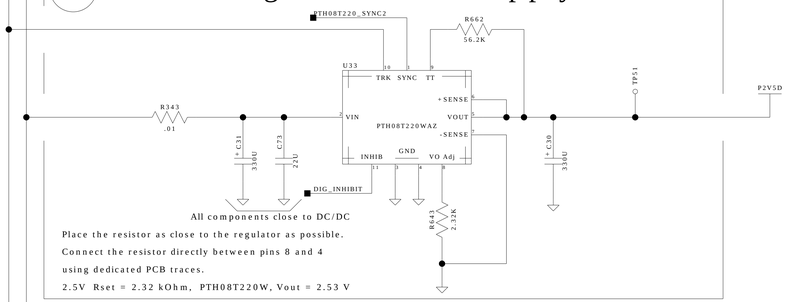


Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 8 and 4
using dedicated PCB traces.
3.3V Rset = 1.21 kOhm, PTH08T220W, Vout = 3.303636 V

G +1.2V Digital Power Supply

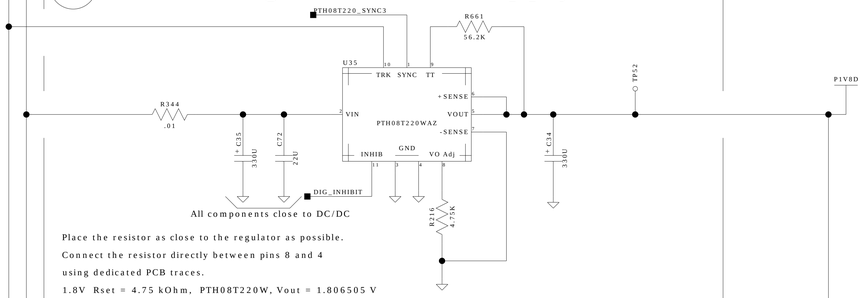


H +2.5V Digital Power Supply



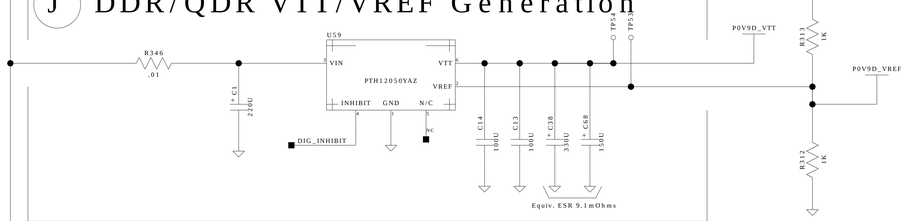
Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 8 and 4
using dedicated PCB traces.
2.5V Rset = 2.32 kOhm, PTH08T220W, Vout = 2.53 V

I +1.8V Digital Power Supply

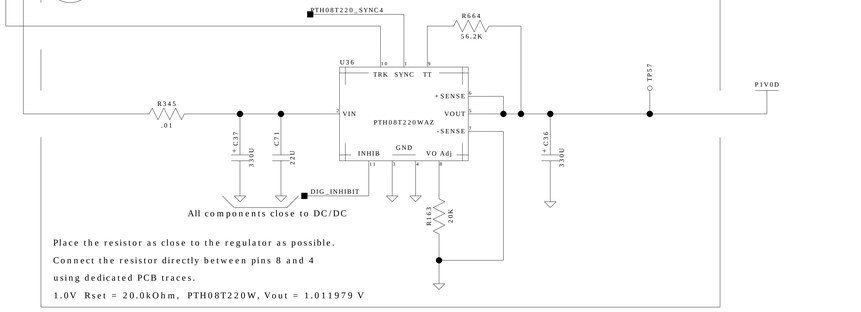


Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 8 and 4
using dedicated PCB traces.
1.8V Rset = 4.75 kOhm, PTH08T220W, Vout = 1.806505 V

J DDR/QDR VTT/VREF Generation

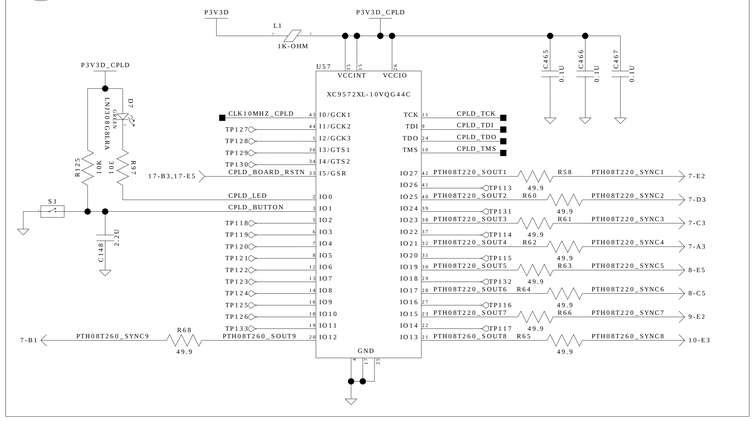


K +1.0V Digital Power Supply

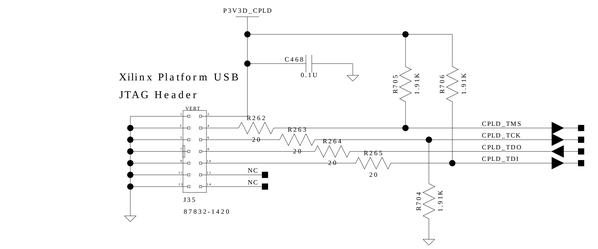


Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 8 and 4
using dedicated PCB traces.
1.0V Rset = 20.0kOhm, PTH08T220W, Vout = 1.011979 V

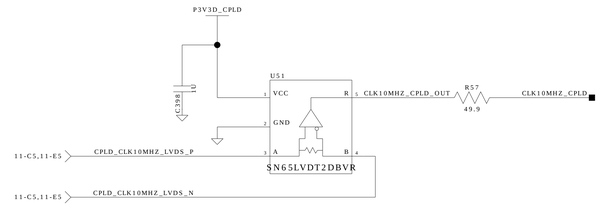
L Sync Generation CPLD



M CPLD JTAG Configuration



N 10MHz Reference LVDS to LVTTL



Digital Power Supply Sequence Order:

1. +12V Input
2. +3.3V
3. +2.5V, +1.8V, +1.2V, +1V, DDR VTT/VREF

VLSI Computation LAB

Title:	XILINX VIRTEX-5 SX50T DIGITAL SUPPLY REGULATION AND SEQUENCING		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
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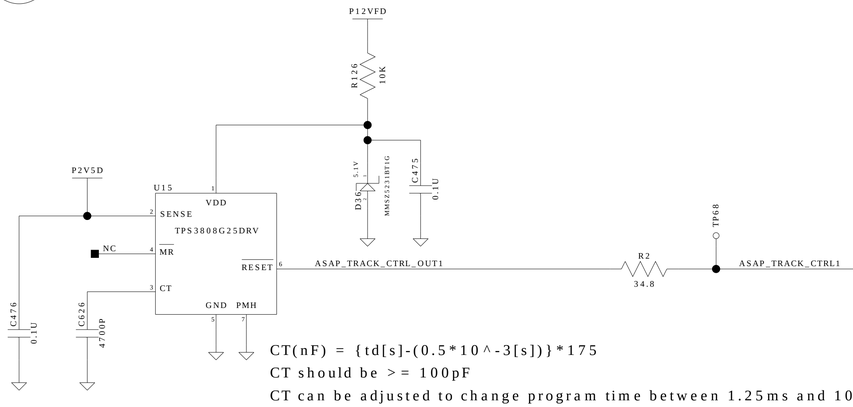
AsAP Digital Power Regulation and Sequencing

Digital Power Supply Sequence Order:

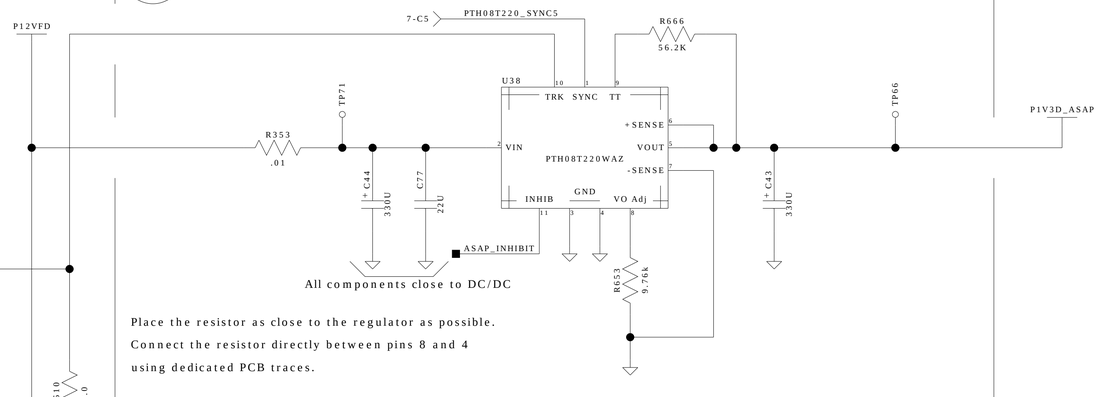
1. +12V Input
2. +3.3V
3. +2.5V
4. +1.3V, +1V

A Digital Supply Sequencer #1



CT(nF) = {td[s]-(0.5*10^-3[s])}*175
CT should be >= 100pF
CT can be adjusted to change program time between 1.25ms and 10s

B +1.3V Digital Power Supply



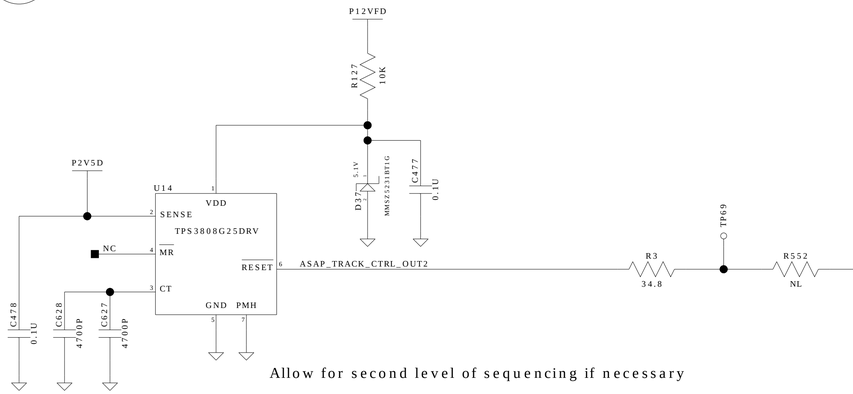
All components close to DC/DC

Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 8 and 4
using dedicated PCB traces.

1.0V Rset = 20.0kOhm, PTH08T220W, Vout = 1.011979 V

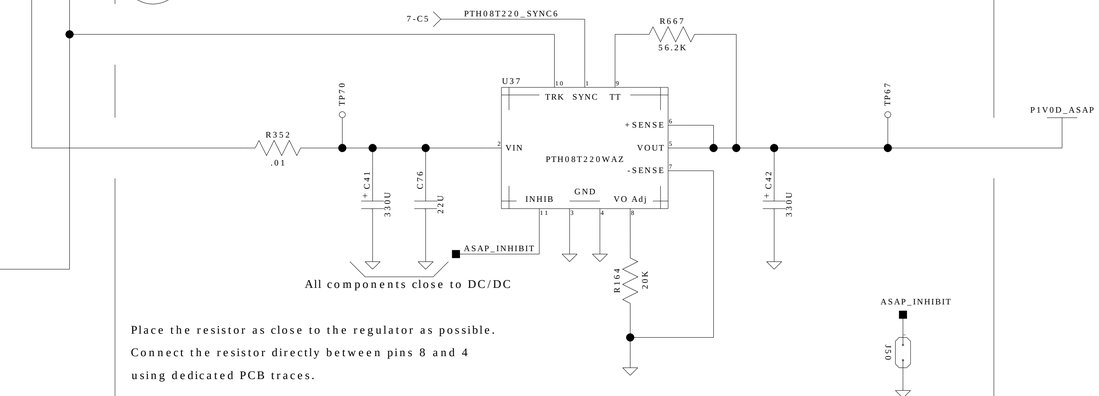
R510
0.0

C Digital Supply Sequencer #2



Allow for second level of sequencing if necessary

D +1.0V Digital Power Supply



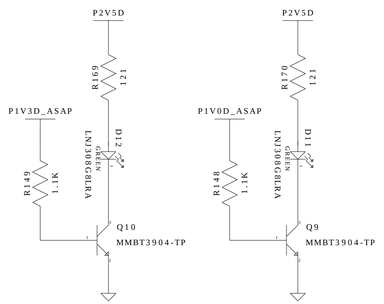
All components close to DC/DC

Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 8 and 4
using dedicated PCB traces.

1.0V Rset = 20.0kOhm, PTH08T220W, Vout = 1.011979 V

Load Jumper to Disable DC/DC Converters

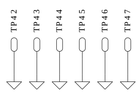
E POWER LEDs



PLACE LEDs NEAR EDGE OF BOARD
Green LED (LNJ308G8LRA):
RLED = (VCC - VF)/IF
VF = 1.9V IF = 5mA

F GROUND Tst Pts

Spread out over board



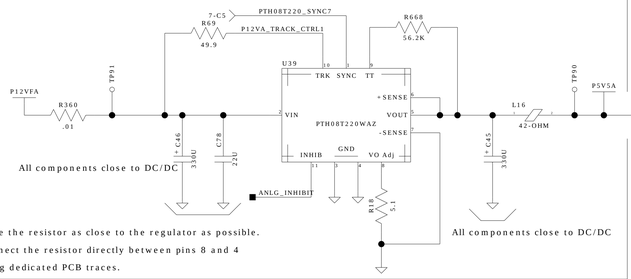
VLSI Computation LAB

Title:	ASAP DIGITAL POWER REGULATION AND SEQUENCING		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: D	Sheet 8 of 43 REV: 001

Analog Power Regulation - Part 1 of 2

A +5.5V Analog Supply Regulation

5.5V Rset = 100 Ohm, PTH08T220W, Vout = 5.498027315 V

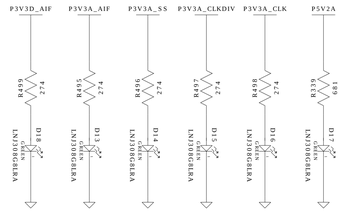


All components close to DC/DC

All components close to DC/DC

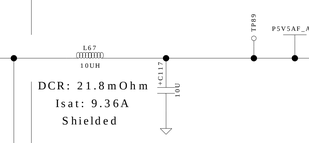
Place the resistor as close to the regulator as possible.
Connect the resistor directly between pins 8 and 4
using dedicated PCB traces.

B POWER LEDs



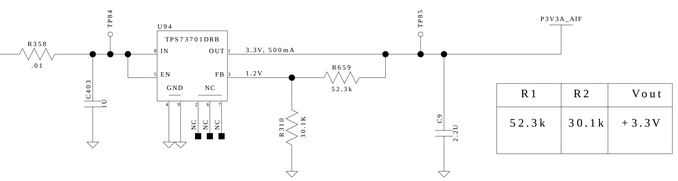
PLACE LEDs NEAR EDGE OF BOARD
Green LED (LNJ308G8LRA):
RLED = (VCC - VF)/IF
VF = 1.9V IF = 5mA

C +5.5V Filter



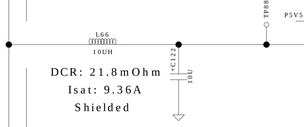
DCR: 21.8mOhm
Isat: 9.36A
Shielded

D +3.3V AIF Analog Supply Regulation



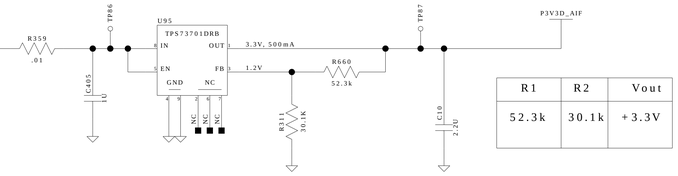
R1	R2	Vout
52.3k	30.1k	+3.3V

E +5.5V Filter



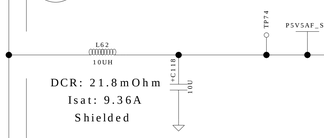
DCR: 21.8mOhm
Isat: 9.36A
Shielded

F +3.3V AIF Digital Supply Regulation



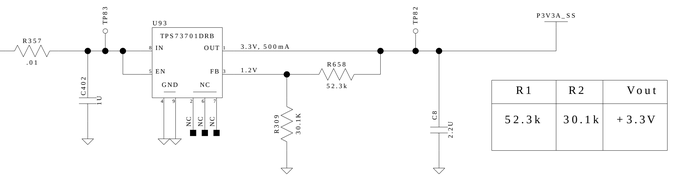
R1	R2	Vout
52.3k	30.1k	+3.3V

G +5.5V Filter



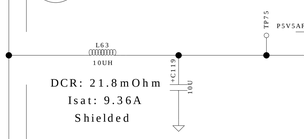
DCR: 21.8mOhm
Isat: 9.36A
Shielded

H +3.3V Signal Source Analog Supply Regulation



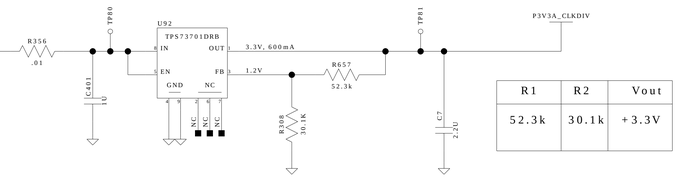
R1	R2	Vout
52.3k	30.1k	+3.3V

I +5.5V Filter



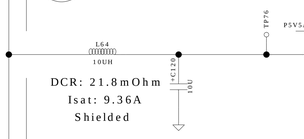
DCR: 21.8mOhm
Isat: 9.36A
Shielded

J +3.3V Clock Divider Analog Supply Regulation



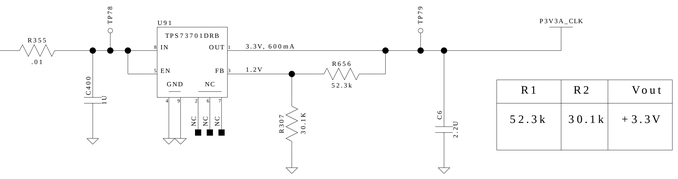
R1	R2	Vout
52.3k	30.1k	+3.3V

K +5.5V Filter



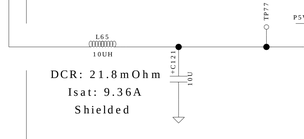
DCR: 21.8mOhm
Isat: 9.36A
Shielded

L +3.3V Clock Analog Supply Regulation



R1	R2	Vout
52.3k	30.1k	+3.3V

M +5.5V Filter

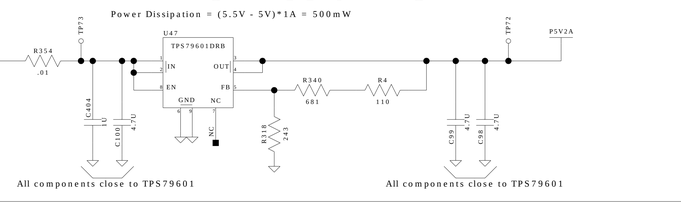


DCR: 21.8mOhm
Isat: 9.36A
Shielded

N +5.2V Analog Supply Regulation

Vout = 1.21 * (1 + (R1/243)) = 5.210849383 V

Power Dissipation = (5.5V - 5V)*1A = 500mW



All components close to TPS79601

All components close to TPS79601

VLSI Computation LAB

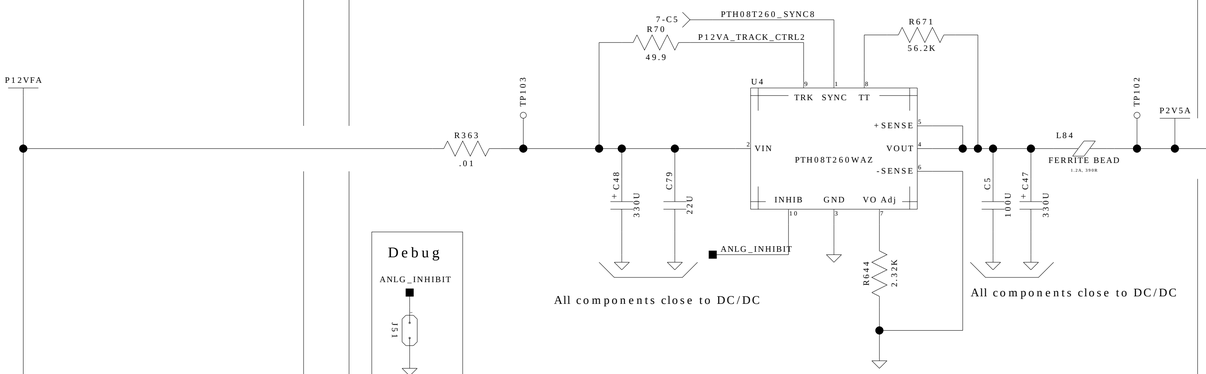
Title:	ANALOG POWER REGULATION - PART 1 OF 2		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 9 of 43	REV: 001

Analog Power Regulation - Part 2 of 2

A +12V Analog

P12VFA

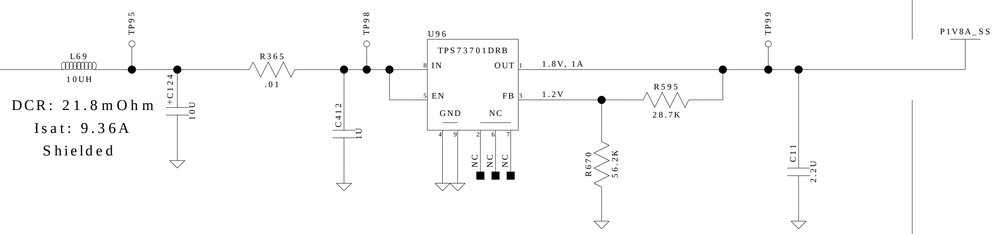
B +2.5V Analog Supply Regulation



2.5V Rset = 2.32 kOhm, PTH08T260W, Vout = 2.53 V

Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 7 and 3 using dedicated PCB traces.

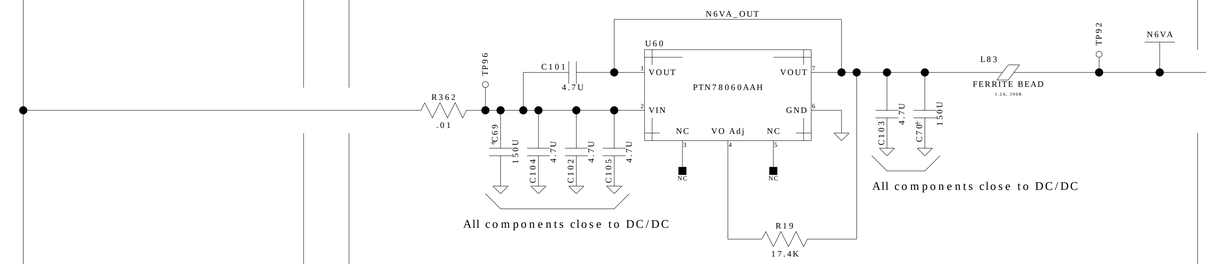
C +1.8V Analog Supply Regulation



DCR: 21.8mOhm
Isat: 9.36A
Shielded

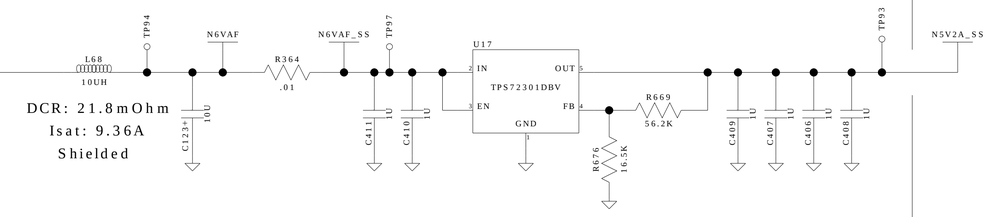
R1	R2	Vout
28.7k	56.2k	+1.818V

D -6V Analog Supply Regulation



-6V Rset = 17.3 kOhm, PTN78060A, Vout = -6V

E -5.2V Analog Supply Regulation



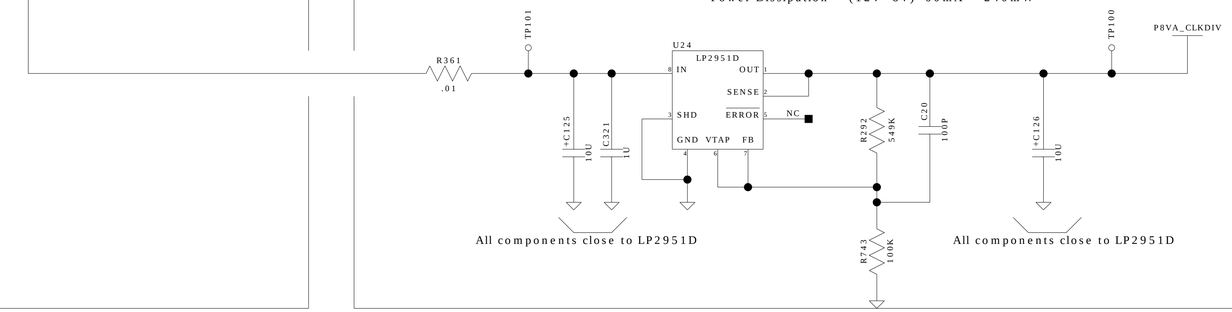
DCR: 21.8mOhm
Isat: 9.36A
Shielded

Vout = -1.186 * (1 + (R1/R2)) = -5.22558788 V

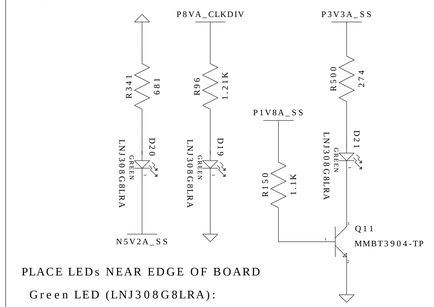
F +8V Analog Supply Regulation

Vout = 1.235 * (1 + (R1/100k)) = 8.01515 V

Power Dissipation = (12V -8V)*60mA = 240mW



G POWER LEDs



PLACE LEDs NEAR EDGE OF BOARD

Green LED (LNJ308G8LRA):

RLED = (VCC - VF)/IF

VF = 1.9V IF = 5mA

VLSI Computation LAB

Title:	ANALOG POWER REGULATION - PART 2 OF 2		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: D	Sheet 10 of 43	REV: 001

10MHz Reference Clock Generation

** INPUTS **

10MHz Control

11-B1,11-C1,11-E1,15-B1 15-D5 → FPGA_CLK10MHZ_REF_CTRL[3:0]

** OUTPUTS **

10MHz Outputs

- FPGA_EXT_CLK10MHZ_REF_P → 11-D5,11-E5,15-D1,15-E1
- FPGA_EXT_CLK10MHZ_REF_N → 11-D5,11-E5,15-D1,15-E1
- FPGA_INT_CLK10MHZ_REF_P → 11-C5,11-E5,15-E1
- FPGA_INT_CLK10MHZ_REF_N → 11-C5,11-E5,15-E1
- CPLD_CLK10MHZ_LVDS_P → 7-A4,11-C5,11-E5
- CPLD_CLK10MHZ_LVDS_N → 7-A4,11-C5,11-E5
- CLK10MHZ_REF_AD9516_P → 11-A2,11-E5,12-D1,12-E1
- CLK10MHZ_REF_AD9516_N → 11-A2,11-E5,12-D1,12-E1
- FPGA_EXT_CLK10MHZ_LOS → 11-B1,11-E5,15-B1,15-D1

A 10 MHz Reference Clock Generation

U78 VTC2-J02C-10M00 TCXO OSC 10.000MHz — VECTRON_10MHZ_REF — R466 0.0 — CLK10MHZ_REF_OSC

U25 Diff/Buffer 3X3mm QFN (VTD, D, DN, VTDN, Q0, Q0N, Q1, Q1N, VCC, VREFAC, VEE)

U21 HCMOS OSC 10MHz (E/D, GND, Vdd, OUT) — FOX_10MHZ_REF — R467 NL

Place Resistors close to eachother to minimize the stub. -OR-

FPGA_CLK10MHZ_REF_CTRL3 INT_CLK10MHZ_ENABLE

CLK10MHZ_INT_BUF_P / CLK10MHZ_INT_BUF_N

U30 SY58017UMG — R317 1K / R316 1K — SEL

U29 SY58017UMG — LAYOUT — CLK10MHZ_REF_P / CLK10MHZ_REF_N

U31 SY58011UMG — R648 1.62K / R647 1.62K — LAYOUT

U28 SY58017UMG — R315 1K / R314 1K

CLK10MHZ_EXT_BUF_P / CLK10MHZ_EXT_BUF_N

J56 142-0701-851 — 10MHz Reference Clock Input — R484 0.0 — R689 33 — D35 PGB10603 — C650 10000P

D48 BAV199DW-7-F — R715 26.1 — T1 MABA-007159-000000

U9 ONET1191PRGTT — R128 10K — C159 0.1U — C25 56P — R672 56.2K — R744 100K

FPGA_EXT_CLK10MHZ_LOS

FPGA_CLK10MHZ_REF_CTRL2 EXT_CLK10MHZ_IN_DISABLE

FPGA_CLK10MHZ_REF_CTRL1 EXT_CLK10MHZ_ENABLE

FPGA_CLK10MHZ_REF_CTRL0 CLK10MHZ_SELECT

FBMJ2125HS420-T (Rated @ 6A) — P3V3A_CLK → L17 42-OHM → P3V3A_10MHZREF — C438 1U

B CML-LVDS Translator

CLK10MHZ_INT_BUF_P / CLK10MHZ_INT_BUF_N

U23 NB4N527S 3X3mm QFN (VTD1, D1, D1, VTD1, VTD0, D0, D0, VTD0, GND, NC, NC, Vcc, Q0, Q0, Q1, Q1)

CLK10MHZ_EXT_BUF_P / CLK10MHZ_EXT_BUF_N

CLK10MHZ_REF_INT_LVDS_P / CLK10MHZ_REF_INT_LVDS_N

FPGA_EXT_CLK10MHZ_REF_P / FPGA_EXT_CLK10MHZ_REF_N

C LVDS 1:2 Fan Out

P2V5D → L132 1K-OHM → P2V5D_10MHZREF

U79 SY58608UMG (IN, NC, Vref-AC, Vt, /IN, Q0, /Q0, Q1, /Q1, GND, PMH, VCC)

CLK10MHZ_REF_INT_LVDS_P / CLK10MHZ_REF_INT_LVDS_N

FPGA_INT_CLK10MHZ_REF_P / FPGA_INT_CLK10MHZ_REF_N

CPLD_CLK10MHZ_LVDS_P / CPLD_CLK10MHZ_LVDS_N

D 10MHz Output Buffer

U76 MC10EP89DTG (VCC, D, D, VEE, Q0, Q0, Q1, Q1)

CLK10MHZ_REF_P / CLK10MHZ_REF_N

CLK10MHZ_REFOUT_P / CLK10MHZ_REFOUT_N

R222 49.9 → CLK10MHZ_REF_AD9516_P

R223 49.9 → CLK10MHZ_REF_AD9516_N

R6 100

C160 0.1U — CLK10MHZ_REF_OUT — R221 49.9 — EXT_CLK10MHZ_REF — R485 0.0 — EXT_CLK10MHZ_REFOUT → J57 142-0701-851 — 10MHz Reference Clock Output

C161 0.1U — R745 100K

R677 75 / R678 75 / R679 75 / R680 75 / R684 75 / R683 75 / R681 75 / R682 75

R7 49.9 / R7 49.9

VLSI Computation LAB

Title:	10MHZ REFERENCE CLOCK GENERATION		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 11 of 43	REV: 001

HIGH-SPEED CLOCK GENERATION

** INPUTS **

AD9516 Control

12-E1,15-C3,15-C5	FPGA_AD9516_SCLK
12-E1,15-C3,15-C5	FPGA_AD9516_CSB
12-E1,15-C3,15-C5	FPGA_AD9516_SDIO
12-E1,15-C3,15-C5	FPGA_AD9516_REF_SEL
12-E1,15-C5,15-E3	FPGA_AD9516_SYNC
12-E1,15-C3,15-C5	FPGA_AD9516_PD
12-E1,15-C3,15-C5	FPGA_AD9516_RESET

10MHz Reference

11-A2,11-E5,12-D1,12-E1	CLK10MHZ_REF_AD9516_P
11-A2,11-E5,12-D1,12-E1	CLK10MHZ_REF_AD9516_N

** OUTPUTS **

High-Speed Clock Outputs (LVPECL)

FPGA_ASAP_CLKIN_P	12-B3,12-E5,22-E1,22-E3
FPGA_ASAP_CLKIN_N	12-B3,12-E5,22-E1,22-E3
FPGA_DSP_CLKIN_P	12-A3,12-E5,22-E1,22-E3
FPGA_DSP_CLKIN_N	12-A3,12-E5,22-E1,22-E3
AIF_ADC_CLKIN_P	12-B2,12-E5,33-C3
AIF_ADC_CLKIN_N	12-B2,12-E5,33-C3
SS_DAC_CLKIN_P	12-A2,12-E5,34-E1
SS_DAC_CLKIN_N	12-A2,12-E5,34-E1

High-Speed Clock Outputs (LVDS)

FPGA_SRAM_CLK_P	12-C3,12-E5,22-E1,22-E3
FPGA_SRAM_CLK_N	12-C3,12-E5,22-E1,22-E3
FPGA_SDRAM_CLK_P	12-C3,12-E5,22-E1,22-E3
FPGA_SDRAM_CLK_N	12-C3,12-E5,22-E1,22-E3
FPGA_IODELAY_CLK_P	12-C3,12-E5,22-D3,22-E1
FPGA_IODELAY_CLK_N	12-C3,12-E5,22-D1,22-D3

AD9516 Control

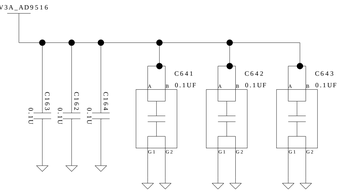
FPGA_AD9516_SDO	12-E5,15-C3,15-D1

AD9516 Status Signals

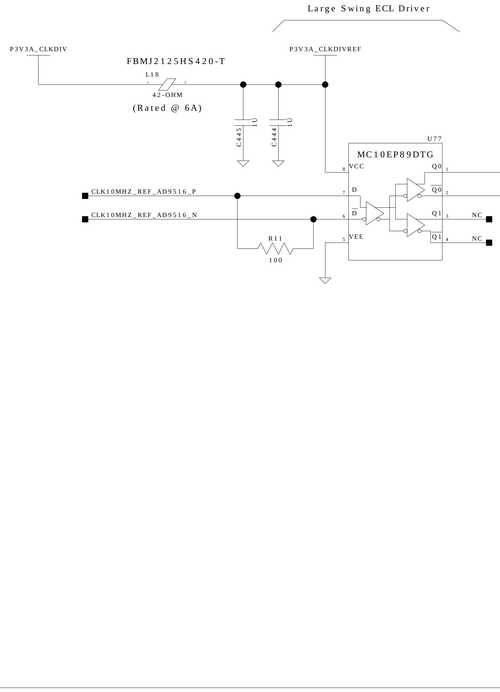
FPGA_AD9516_STATUS	12-E5,15-C3,15-D1
FPGA_AD9516_REFMON	12-E5,15-C3,15-D1
FPGA_AD9516_LD	12-D5,15-C3,15-D1

A AD9516 LVPECL Power Supply Decoupling

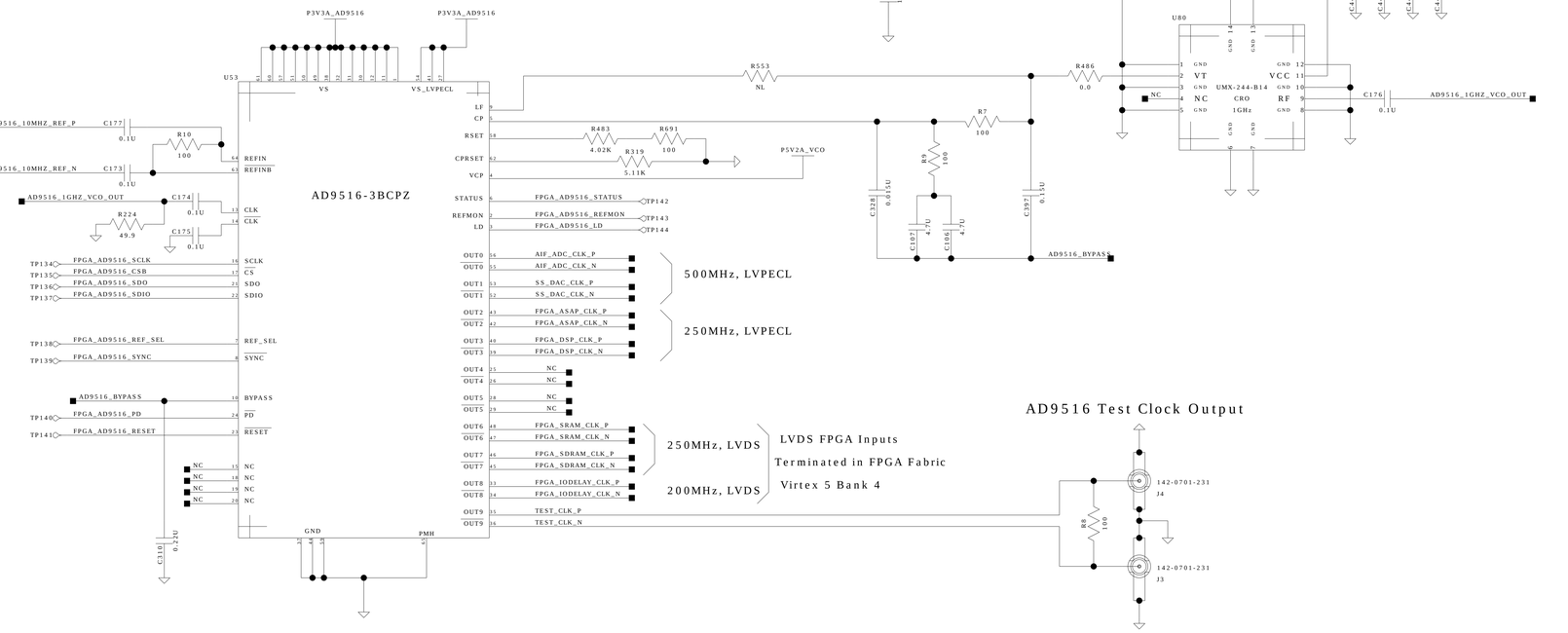
+2.5V Clock: I = 300mA max



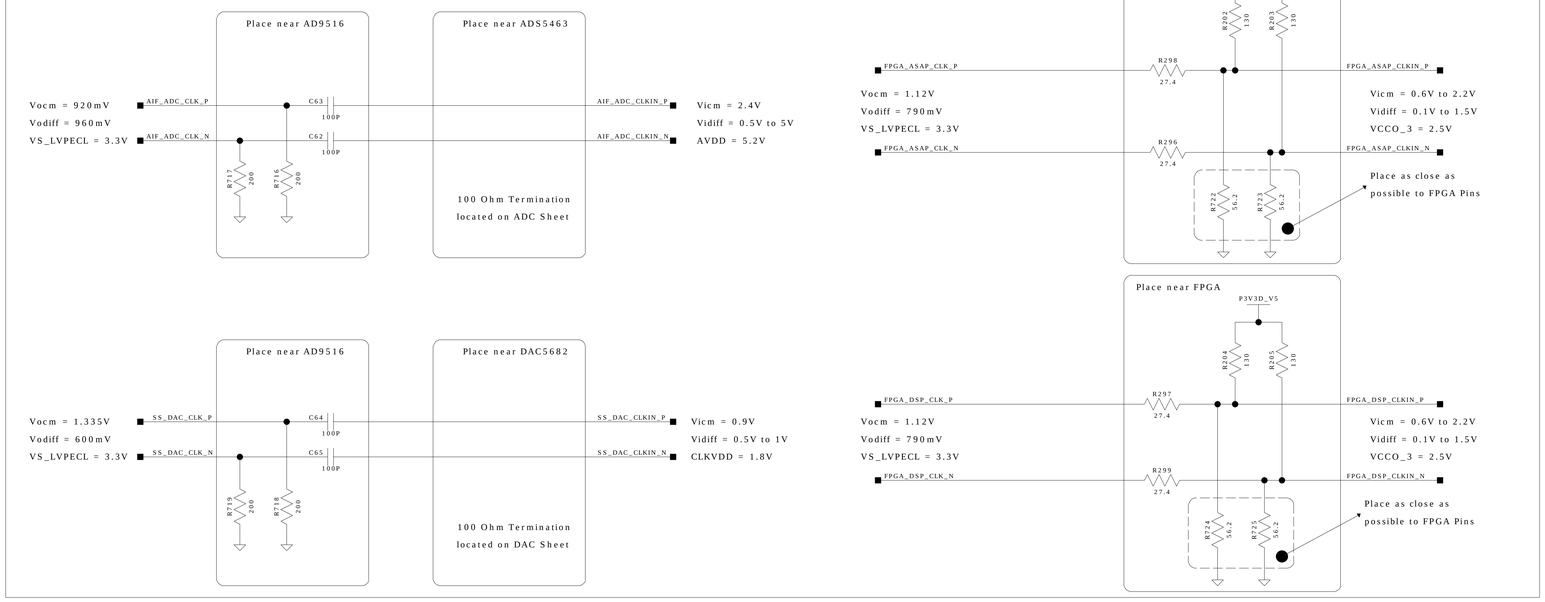
B 10 MHz Reference Clock Buffer



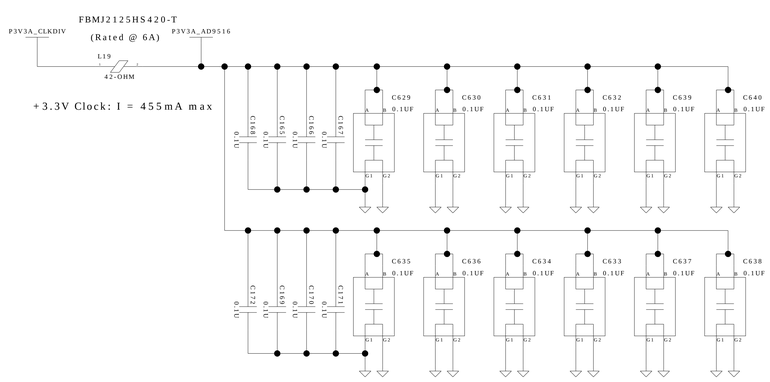
C AD9516 High-Speed Clock Generation PLL



D AD9516 LVPECL Clock Terminations



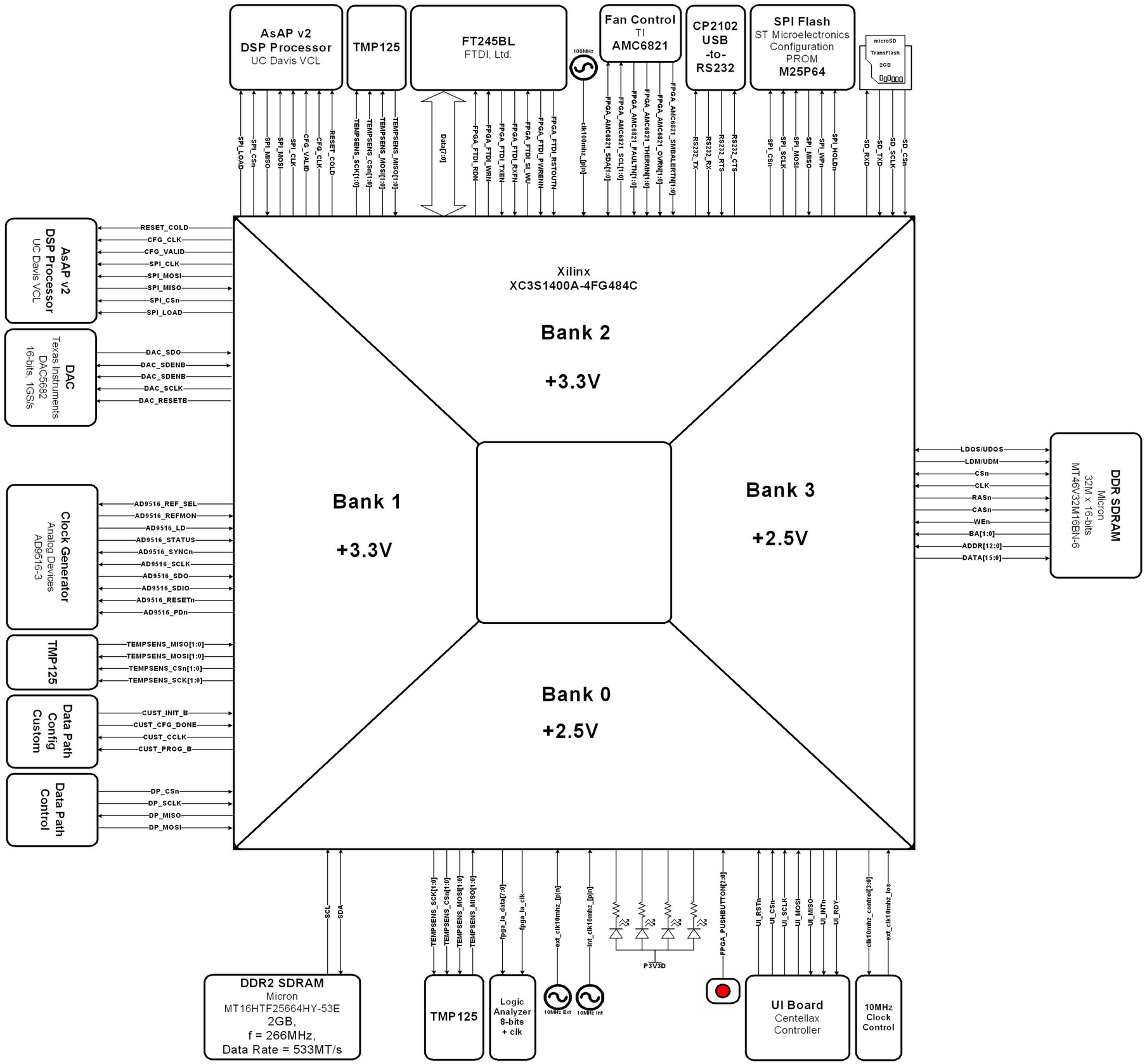
E AD9516 Main Power Supply Decoupling



VLSI Computation LAB

Title:	HIGH-SPEED CLOCK GENERATION		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 12 of 43 REV: 001

Control FPGA Digital Design



VLSI Computation LAB

Title:	CONTROL FPGA DIGITAL DESIGN		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 13 of 43 REV: 001

Xilinx Spartan-3A Control FPGA Configuration

** INPUTS **

CPU Interrupts

14-D2,14-E1,17-A2,17-D5 — FPGA_UI_PROG0

AMC6821 Fan #2 Control

6-B1,14-D4,14-E1 — FPGA_AMC6821_FAN2_OVRN

** OUTPUTS **

CPU Interrupts

FPGA_UI_PROG1 — 14-D2,14-E5,17-A2,17-E1

FPGA_UI_PROG2 — 14-E3,14-E5,17-A2,17-E1

AMC6821 Fan #2 Control

FPGA_AMC6821_FAN2_SDA — 6-A4,14-D4,14-E5

FPGA_AMC6821_FAN2_SCK — 6-A4,14-D4,14-E5

FT245BL USB Interface

FPGA_FTDI_RDN — 14-D4,14-E5,17-D5,17-D1

AsAP 2 Config Input

FPGA_ASAP2_RST_CNTCLK — 14-D4,14-E5,40-B5,40-E1

Temp Sensor Col. 1

FPGA_TMPSENS_1C_CSN — 14-D4,14-E5,20-E1,20-E2

A Configuration SPI Flash PROM / JTAG Interface

Spartan 3A: VCCO_2 = 3.3V, VCCAUX = 3.3V
Virtex 5 SX50T: VCCO_0 = 3.3V, VCCO_2 = 3.3V

Place Green and Red LED next to eachother with Silkscreen Labels.

Holds off configuration while low.
Configuration starts on rising edge.

PUSH TO RE-PROGRAM

Xilinx Platform USB JTAG Header

Xilinx Platform USB SPI Header

U19 XC3S1400A-4FG484C (4 of 4)

S3A_CONFIG_DONE	Y19	DONE/VCCAUX
S3A_PROG_B	C4	PROG_B/VCCAUX
TMS	D4	TMS/VCCAUX
TCK	A21	TCK/VCCAUX
TDI_TO_V5	E19	TDO/VCCAUX
TDI_TO_S3A	F5	TDI/VCCAUX
S3A_M0	W5	IO_L01N_2/M0
S3A_M1	V6	IO_L01P_2/M1
S3A_M2	W4	IO_L02P_2/M2
S3A_V0	Y8	IO_L11N_2/VS0
S3A_V1	W8	IO_L11P_2/VS1
S3A_V2	W9	IO_L09N_2/VS2
S3A_INIT_B	V13	IO_L26P_2/INIT_B
S3A_SPI_CSO	Y4	IO_L02N_2/CSO_B
S3A_CCLK	AA20	IO_L36N_2/CCLK
S3A_SPI_MOSI	AB14	IO_L22N_2/MOSI/CSI_B
FPGA_AMC6821_FAN2_SDA	Y9	IO_L14P_2/D7
FPGA_AMC6821_FAN2_SCK	AB9	IO_L14N_2/D6
NC	Y11	IO_L16P_2/D5
NC	AB11	IO_L16N_2/D4
FPGA_FTDI_RDN	U13	IO_L26N_2/D3
FPGA_ASAP2_RST_CNTCLK	AA17	IO_L28P_2/D2
FPGA_TMPSENS_1C_CSN	Y17	IO_L28N_2/D1
S3A_SPI_MISO	AB20	IO_L36P_2/D0/DIN/MISO
FPGA_AMC6821_FAN2_OVRN	V9	IO_L09P_2/RDWR_B
S3A_SPI_DATA_TO_V5	AA15	IO_L24N_2/DOUT

MASTER JTAG CHAIN MAPPING	
FROM	TO
JTAG Cable	S3A Control
S3A Control	V5 Data
V5 Data	JTAG Cable

NOTES:
FPGA_CCLK requires an end termination and is a 50 Ohm controlled impedance transmission line.The end termination must be placed near the Configuration PROM.
FPGA_CCLK Stub Length from S3A to SPI Flash < 12.5 mm

B Spartan-3A FPGA CONFIG MODE

For more information see Xilinx Spartan 3A Configuration Guide (UG332)

CONFIG MODE	M2	M1	M0	DATA WIDTH	CCLK Direction
Master Serial	0	0	0	1 bit	Output
Master SPI	0	0	1	1 bit	Output
Master BPI-Up	0	1	0	8, 16 bits	Output
RSVD	0	1	1	RSVD	RSVD
RSVD	1	0	0	RSVD	RSVD
JTAG	1	0	1	1 bit	Input (TCK)
Slave Parallel	1	1	0	8, 16, 32 bits	Input
Slave Serial	1	1	1	1 bit	Input

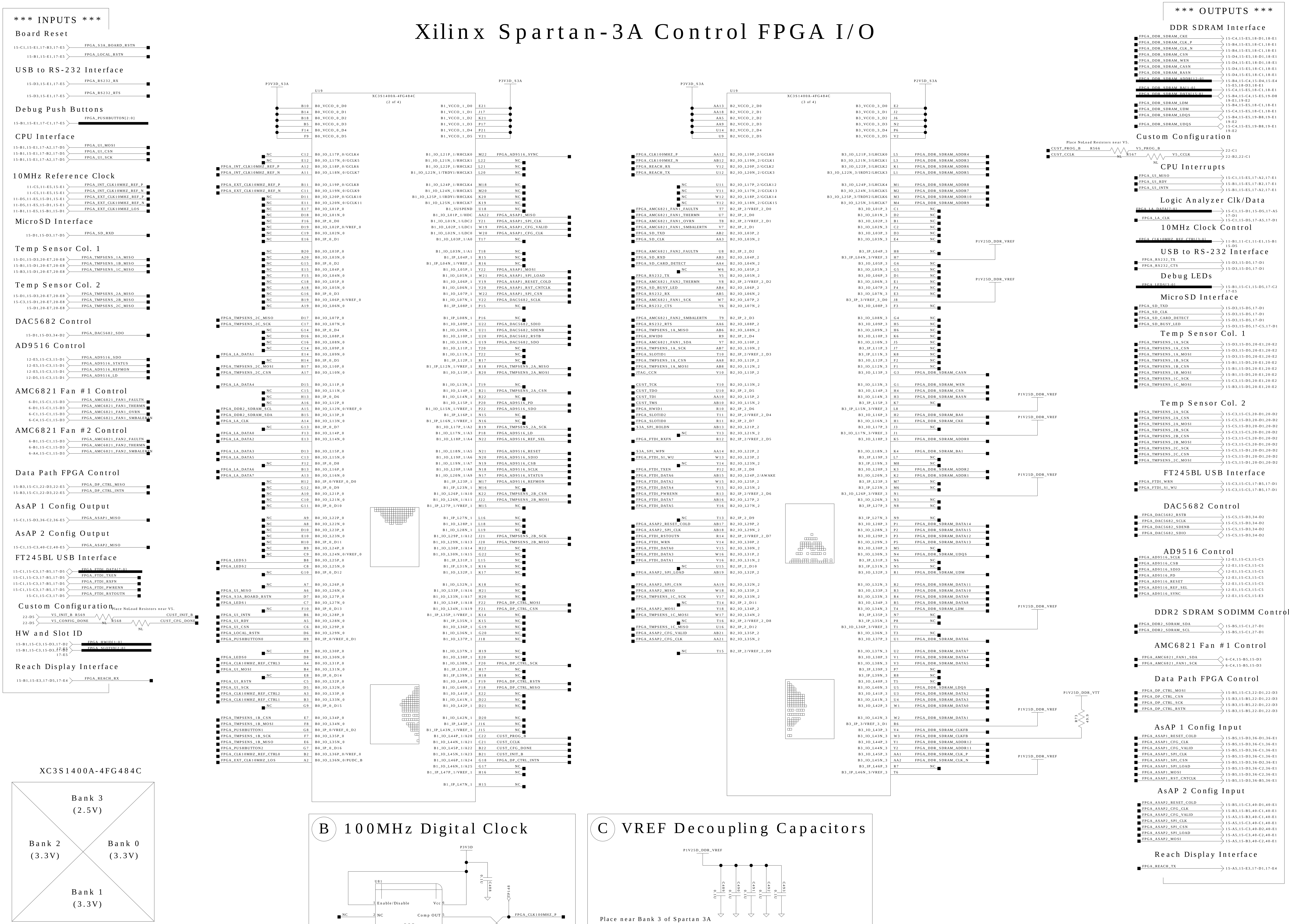
C Spartan-3A FPGA SPI MODE

VS2	VS1	VS0	READ CMD	HEX CMD CODE
1	1	1	Fast Read	0x0B
1	0	1	Read	0x03
1	1	0	Read Array	0xE8
OTHERS			RESERVED	

VLSI Computation LAB

Title:	XILINX SPARTAN-3A CONTROL FPGA CONFIGURATION		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 14 of 43	REV: 001

Xilinx Spartan-3A Control FPGA I/O

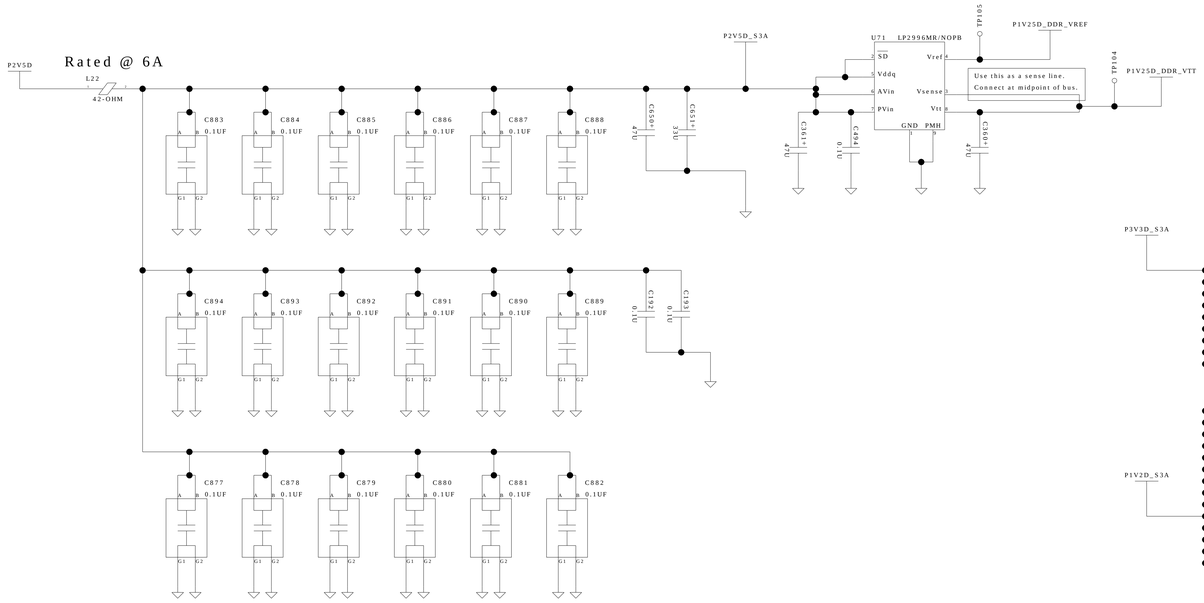


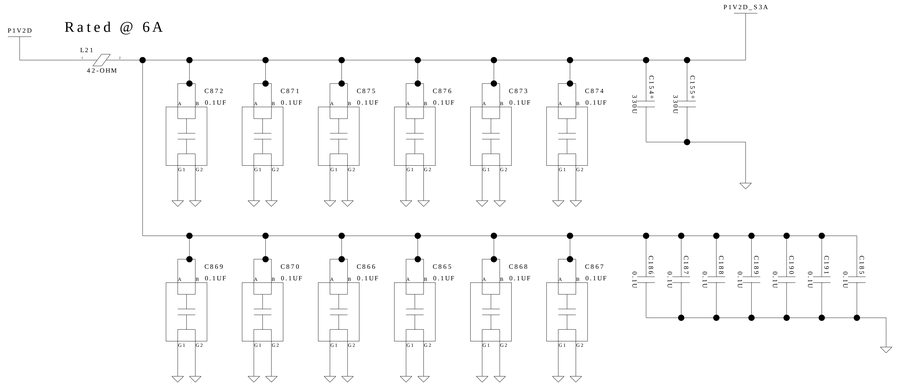
Bank 0 (3.3V): Clock Path FPGA/Logic Analyzer
Bank 1 (3.3V): SPI Device Interfaces
Bank 2 (3.3V): SPI Device Interfaces
Bank 3 (2.5V): uBlaze SDRAM

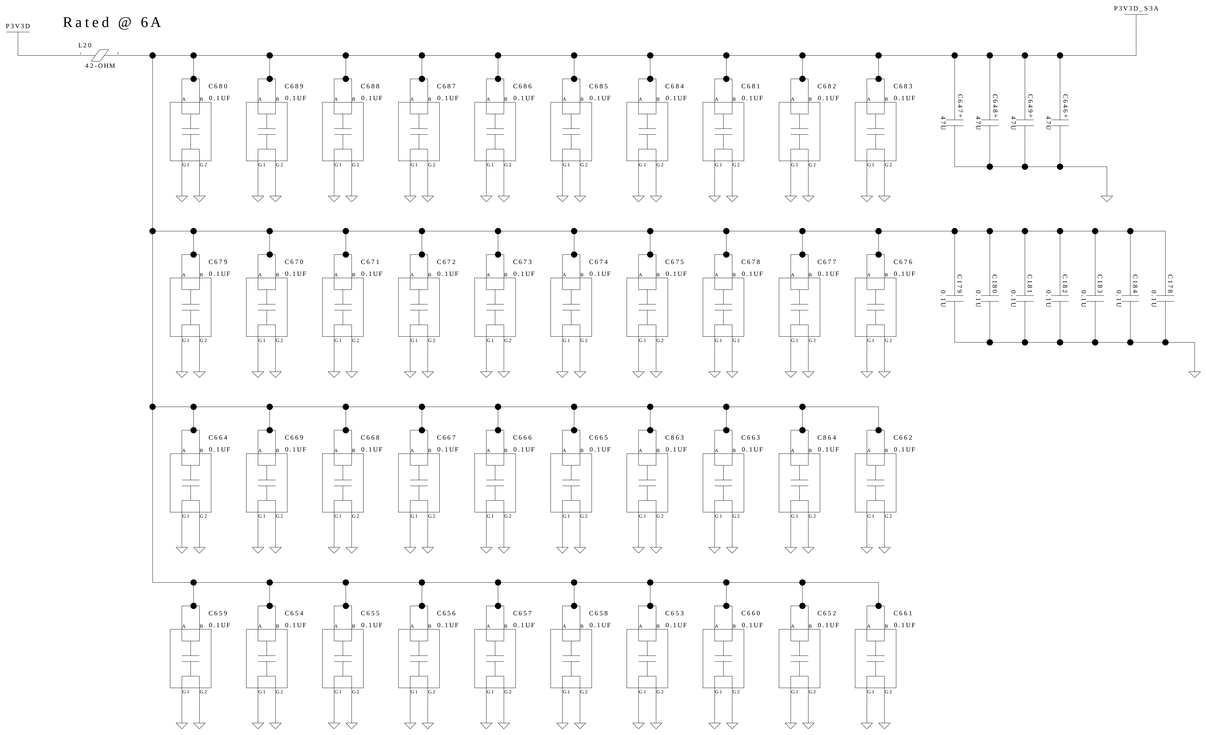
VLSI Computation LAB

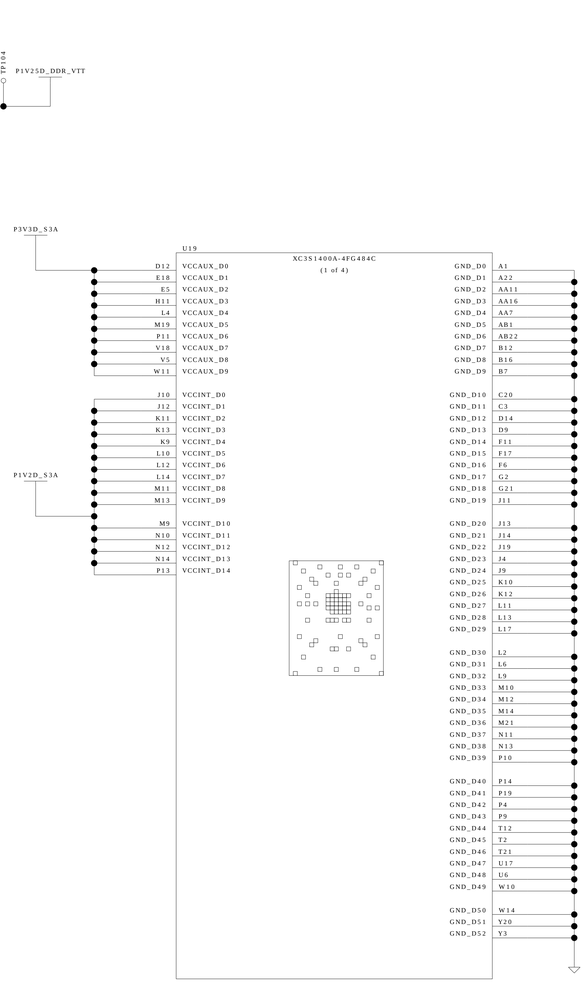
Title:	XILINX SPARTAN-3A CONTROL FPGA I/O		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 15 of 43 REV: 001

Xilinx Spartan-3A Control FPGA Power Supplies

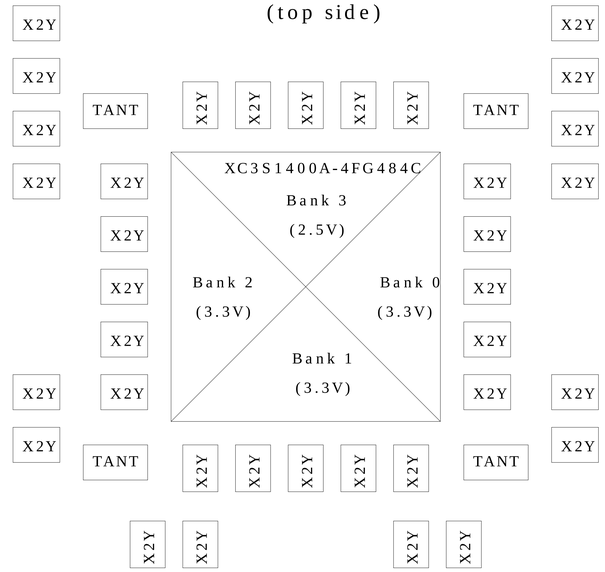




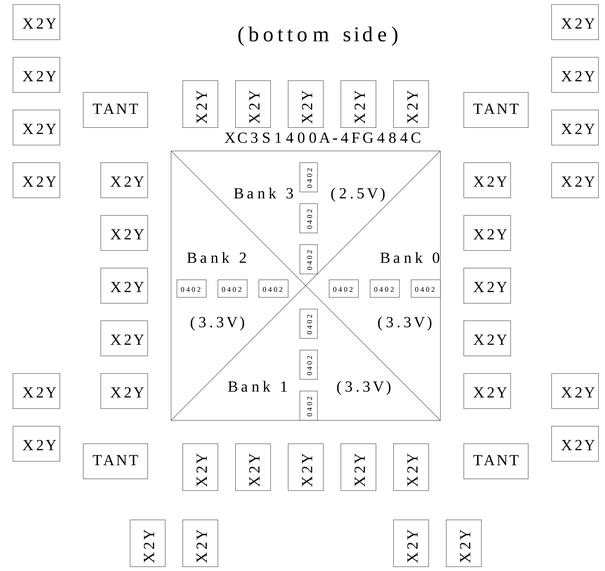




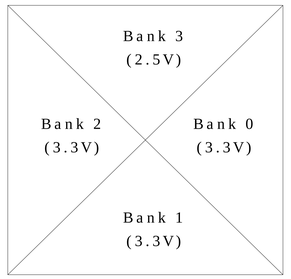
Capacitor Placement (top side)



Capacitor Placement (bottom side)



XC3S1400A-4FG484C



Bank 0 (3.3V): UI, 10MHz, LEDs, ...
Bank 1 (3.3V): SPI Device Interfaces
Bank 2 (3.3V): FTDI, AsAP #2, microSD, Fan Ctrl, ...
Bank 3 (2.5V): uBlaze SDRAM

X2Y Capacitor Via Placement

Tantalum/O402 Via Placement

VLSI Computation LAB

Title:	XILINX SPARTAN-3A CONTROL FPGA POWER SUPPLIES		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 16 of 43	REV: 001

Xilinx Spartan-3A Control FPGA Peripherals

*** INPUTS ***

CPU Interrupts

15-C1,15-E5,17-A2,17-E1	FPGA_UI_MISO
15-B1,15-E5,17-B2,17-E1	FPGA_UI_RDY
15-B1,15-E5,17-A2,17-E1	FPGA_UI_INTN
14-D2,14-E5,17-A2,17-E1	FPGA_UI_PROG1
14-E3,14-E5,17-A2,17-E1	FPGA_UI_PROG2

SDRAM Data/Address/Ctrl

17-D3,17-E1,18-D3,18-E5	DDR_SDRAM_CKE
17-D3,17-E1,18-C3,18-E5	DDR_SDRAM_CLK_P
17-D3,17-E1,18-C3,18-E5	DDR_SDRAM_CLK_N
17-D3,17-E1,18-C3,18-E5	DDR_SDRAM_CSN
17-D3,17-E1,18-D3,18-E5	DDR_SDRAM_WEN
17-D3,17-E1,18-D3,18-E5	DDR_SDRAM_CASN
17-D3,17-E1,18-C3,18-E5	DDR_SDRAM_RASN
17-C4,17-E1,18-C3,18-E5	DDR_SDRAM_LDM
17-C4,17-E1,18-C3,18-E5	DDR_SDRAM_UDM
17-C4,17-E1,19-B1,19-E7 19-E8	DDR_SDRAM_LDQS
17-C4,17-E1,19-B1,19-E7 19-E8	DDR_SDRAM_UDQS
17-C3,17-D3,17-E1,18-C5 18-D5,18-E5	DDR_SDRAM_ADDR[12:0]
17-C3,17-E1,18-C3,18-E5	DDR_SDRAM_BA[1:0]
17-C4,17-D4,17-E1,19-D1 19-E7,19-E8	DDR_SDRAM_DATA[15:0]

Logic Analyzer Clk/Data

15-C1,15-D1,15-D5,17-A5 17-D1	FPGA_LA_DATA[7:0]
15-C1,15-D5,17-A5,17-D1	FPGA_LA_CLK

MicroSD Interface

15-D3,15-D5,17-D1	FPGA_SD_TXD
15-D3,15-D5,17-D1	FPGA_SD_CLK
15-D3,15-D5,17-D1	FPGA_SD_CARD_DETECT
15-D3,15-D5,17-C5,17-D1	FPGA_SD_BUSY_LED

USB to RS-232

15-D3,15-D5,17-D1	FPGA_RS232_TX
15-D3,15-D5,17-D1	FPGA_RS232_CTS

FT245BL USB Interface

14-D4,14-E5,17-B5,17-D1	FPGA_FTDI_RDN
15-C3,15-C5,17-B5,17-D1	FPGA_FTDI_WRN
15-C3,15-C5,17-B5,17-D1	FPGA_FTDI_SI_WU

Reach Display Interface

15-A5,15-E3,17-D1,17-E4	FPGA_REACH_TX

*** OUTPUTS ***

Clock Path Board Reset

FPGA_LOCAL_RSTN	15-B1,15-E1,17-E5
FPGA_S3A_BOARD_RSTN	15-C1,15-E1,17-B3,17-E5
FPGA_V5_BOARD_RSTN	17-B3,17-E5,22-C1,22-D3
CPLD_BOARD_RSTN	7-D4,17-B3,17-E5

USB to RS-232 Interface

FPGA_RS232_RTS	15-D3,15-E1,17-E5
FPGA_RS232_RX	15-D3,15-E1,17-E5

HW and Slot ID

FPGA_HWID[1:0]	15-B1,15-C3,15-D3,17-D2
FPGA_SLOTID[2:0]	15-B1,15-C3,15-D3,17-D2 17-E5

Debug LEDs

FPGA_LEDS[3:0]	15-B1,15-C1,15-D5,17-C2 17-E5

Debug Push Buttons

FPGA_PUSHBUTTON[2:0]	15-B1,15-E1,17-C1,17-E5

CPU Interface

FPGA_UI_MOSI	15-B1,15-E1,17-A2,17-D5
FPGA_UI_CSN	15-B1,15-E1,17-B2,17-D5
FPGA_UI_SCK	15-B1,15-E1,17-A2,17-D5
FPGA_UI_PROG0	14-D2,14-E1,17-A2,17-D5

MicroSD Interface

FPGA_SD_RXD	15-D1,15-D3,17-D5

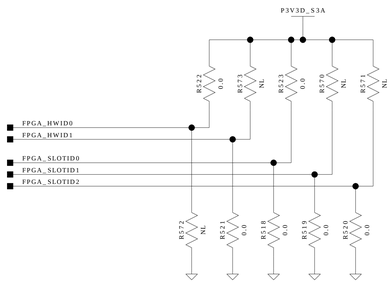
FT245BL USB Interface

FPGA_FTDI_DATA[7:0]	15-C1,15-C3,17-B5,17-D5
FPGA_FTDI_TXEN	15-C1,15-C3,17-B5,17-D5
FPGA_FTDI_RXFN	15-C1,15-C3,17-B5,17-D5
FPGA_FTDI_PWRENN	15-C1,15-C3,17-B5,17-D5
FPGA_FTDI_RSTOUTN	15-C1,15-C3,17-D5

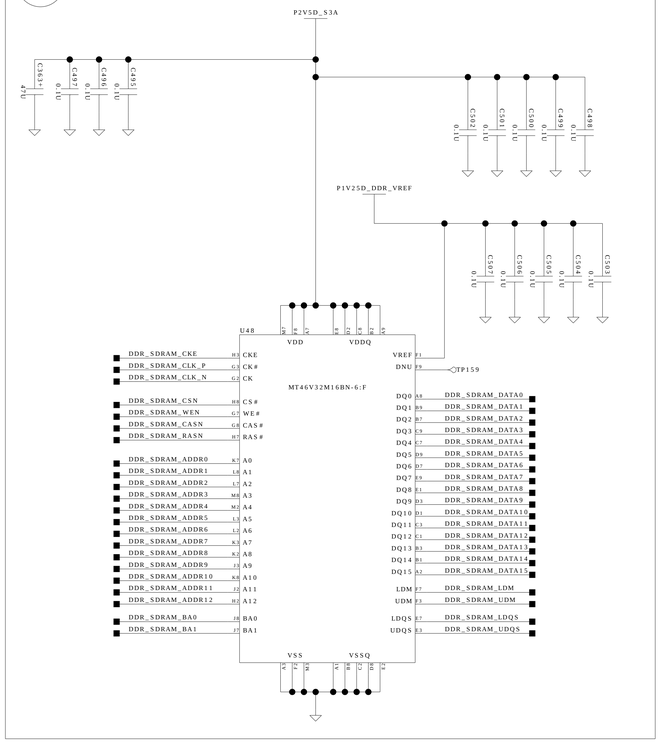
Reach Display Interface

FPGA_REACH_RX	15-B1,15-E3,17-D5,17-E4

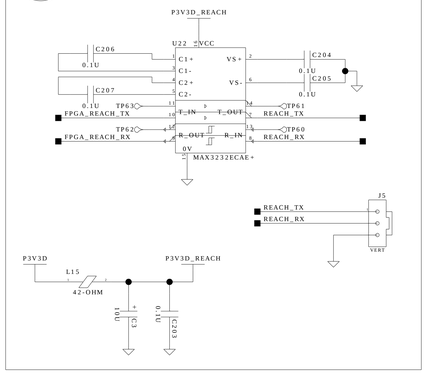
A HW and Slot ID



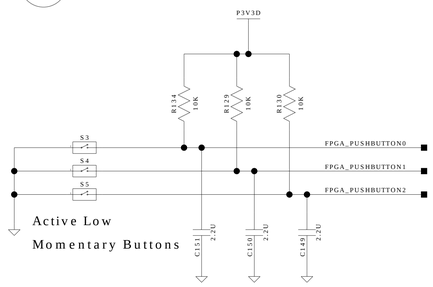
B DDR SDRAM



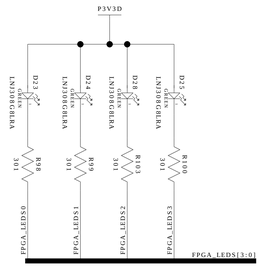
C Reach Display



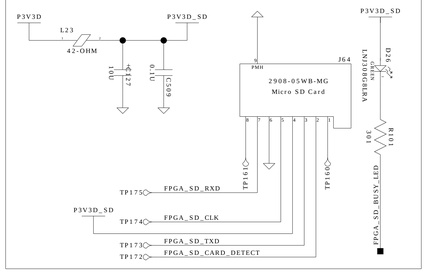
D PUSH-BUTTONs



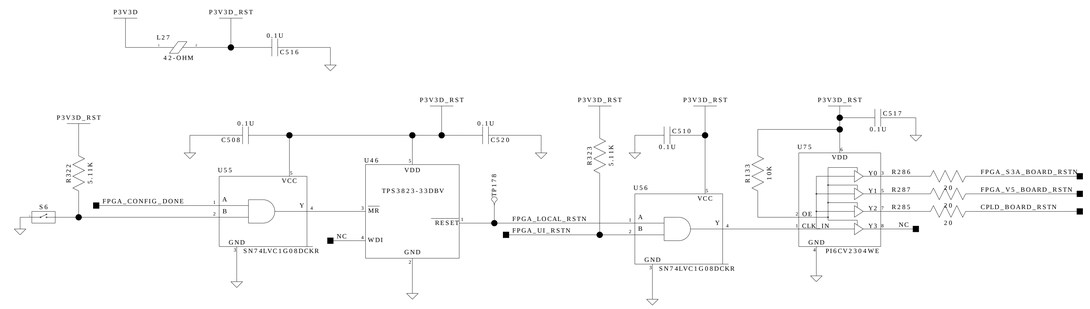
E DEBUG LEDs



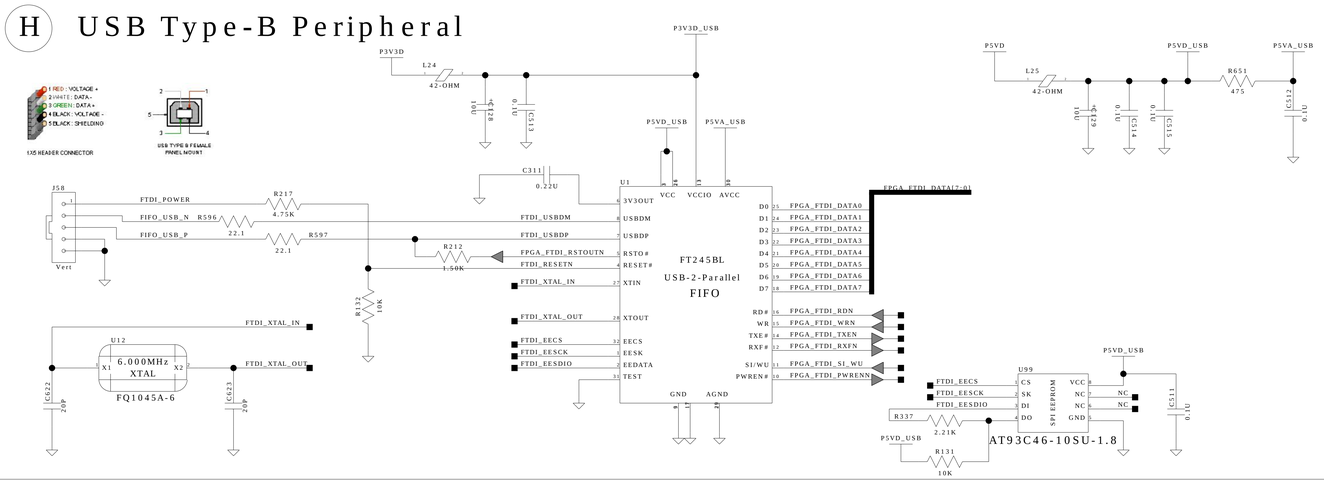
F micro SD Card (2GB)



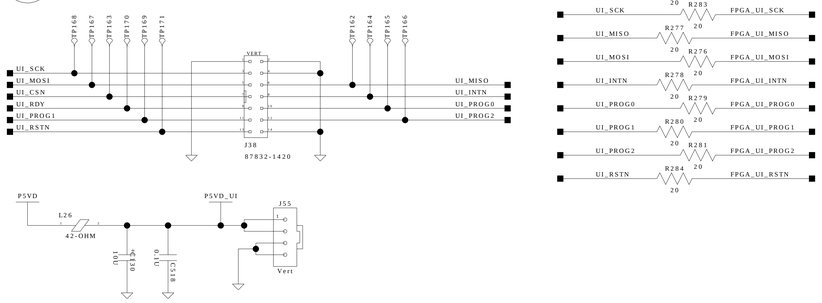
G Reset Circuit



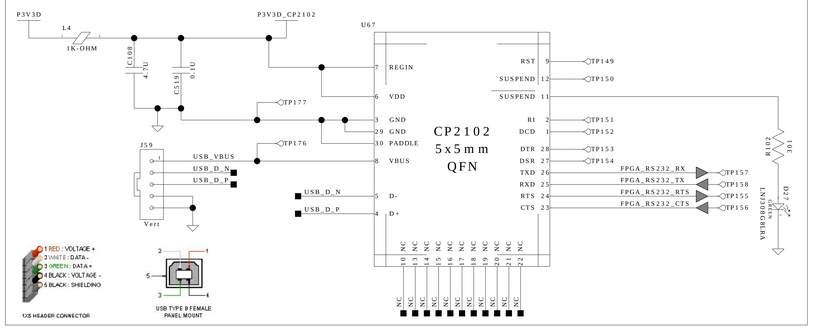
H USB Type-B Peripheral



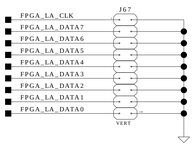
I User Interface Board



J USB-to-RS-232 Debug Interface



K LOGIC ANALYZER HEADER



VLSI Computation LAB

Title:	XILINX SPARTAN-3A CONTROL FPGA PERIPHERALS		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 17 of 43 REV: 001

DDR SDRAM Address and Control Terminations

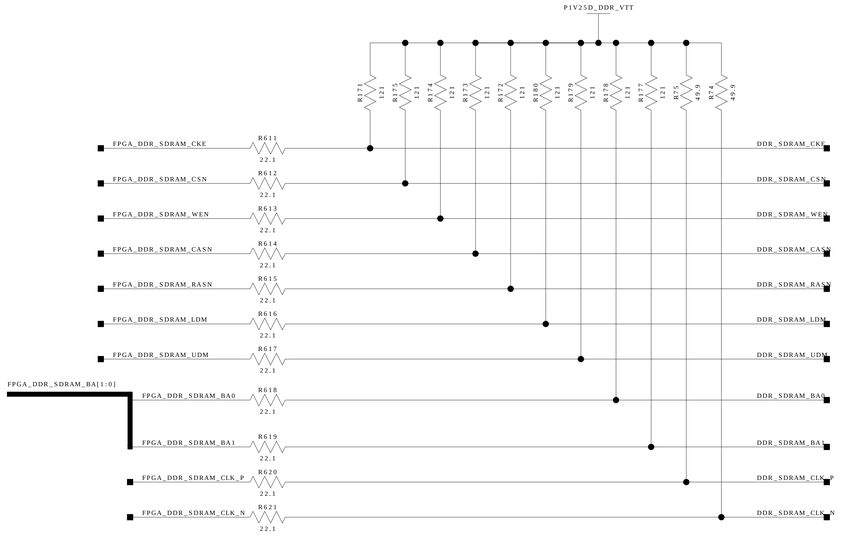
*** INPUTS ***

15-C4,15-E5,18-D1,18-E1 — FPGA_DDR_SDRAM_CKE
15-B4,15-E5,18-C1,18-E1 — FPGA_DDR_SDRAM_CLK_P
15-B4,15-E5,18-C1,18-E1 — FPGA_DDR_SDRAM_CLK_N
15-D4,15-E5,18-D1,18-E1 — FPGA_DDR_SDRAM_CSN
15-D4,15-E5,18-D1,18-E1 — FPGA_DDR_SDRAM_WEN
15-D4,15-E5,18-C1,18-E1 — FPGA_DDR_SDRAM_CASN
15-D4,15-E5,18-C1,18-E1 — FPGA_DDR_SDRAM_RASN
15-B4,15-C4,15-D4,15-E4 15-E5,18-D3,18-E1 — FPGA_DDR_SDRAM_ADDR[12:0]
15-C4,15-E5,18-C1,18-E1 — FPGA_DDR_SDRAM_BA[1:0]
15-B4,15-E5,18-C1,18-E1 — FPGA_DDR_SDRAM_LDM
15-C4,15-E5,18-C1,18-E1 — FPGA_DDR_SDRAM_UDM

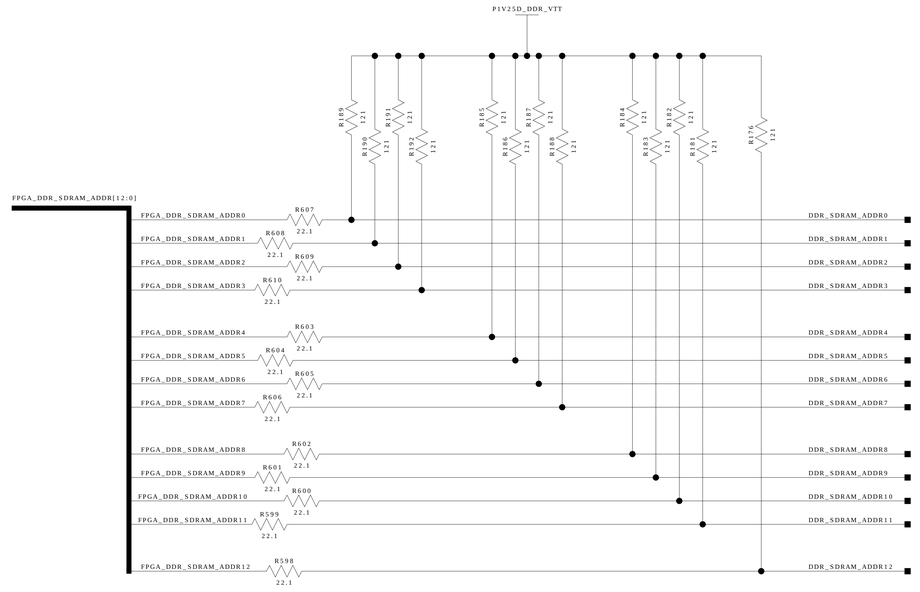
*** OUTPUTS ***

DDR_SDRAM_CKE — 17-D3,17-E1,18-D3,18-E5
DDR_SDRAM_CLK_P — 17-D3,17-E1,18-C3,18-E5
DDR_SDRAM_CLK_N — 17-D3,17-E1,18-C3,18-E5
DDR_SDRAM_CSN — 17-D3,17-E1,18-D3,18-E5
DDR_SDRAM_WEN — 17-D3,17-E1,18-D3,18-E5
DDR_SDRAM_CASN — 17-D3,17-E1,18-C3,18-E5
DDR_SDRAM_RASN — 17-D3,17-E1,18-C3,18-E5
DDR_SDRAM_ADDR[12:0] — 17-C3,17-D3,17-E1,18-C5 18-D5,18-E5
DDR_SDRAM_BA[1:0] — 17-C3,17-E1,18-C3,18-E5
DDR_SDRAM_LDM — 17-C4,17-E1,18-C3,18-E5
DDR_SDRAM_UDM — 17-C4,17-E1,18-C3,18-E5

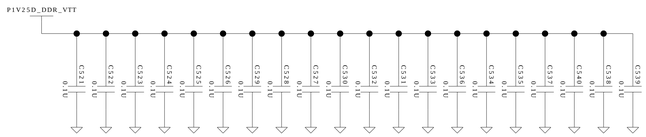
A DDR SDRAM Control Terminations



B DDR SDRAM Address Terminations



C VTT Termination Decoupling Capacitors

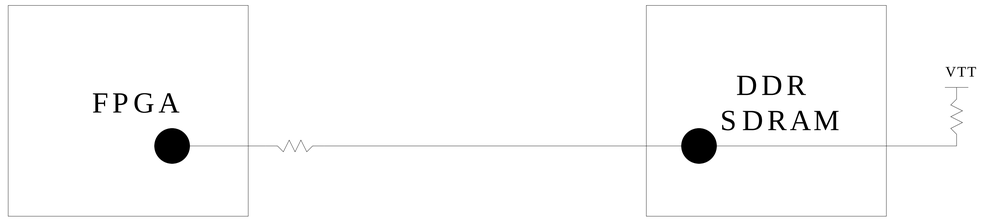


Place near DDR SDRAM Terminations

Address/Control Termination Placement:

Place parallel terminations just beyond the SDRAM.

Place the series terminations close to the Spartan 3A FPGA



VLSI Computation LAB

Title:	DDR SDRAM ADDRESS AND CONTROL TERMINATIONS		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 18 of 43	REV: 001

DDR SDRAM Data Terminations

*** INPUTS ***

15-B4,15-C4,15-E5,19-D8 19-E2 — FPGA_DDR_SDRAM_DATA[15:0]
15-B4,15-E5,19-B8,19-E2 — FPGA_DDR_SDRAM_LDQS
15-C4,15-E5,19-B8,19-E2 — FPGA_DDR_SDRAM_UDQS

*** OUTPUTS ***

DDR_SDRAM_DATA[15:0] — 17-C4,17-D4,17-E1,19-D1 19-E7
DDR_SDRAM_LDQS — 17-C4,17-E1,19-B1,19-E7
DDR_SDRAM_UDQS — 17-C4,17-E1,19-B1,19-E7

P1V25D_DDR_VTT

R260 49.9, R259 49.9, R240 49.9, R239 49.9, R238 49.9, R237 49.9, R233 49.9, R234 49.9, R235 49.9, R236 49.9, R229 49.9, R230 49.9, R231 49.9, R232 49.9, R228 49.9, R227 49.9, R226 49.9, R225 49.9

P1V25D_DDR_VTT

R258 49.9, R257 49.9, R244 49.9, R243 49.9, R242 49.9, R241 49.9, R248 49.9, R247 49.9, R246 49.9, R245 49.9, R252 49.9, R251 49.9, R250 49.9, R249 49.9, R256 49.9, R255 49.9, R254 49.9, R253 49.9

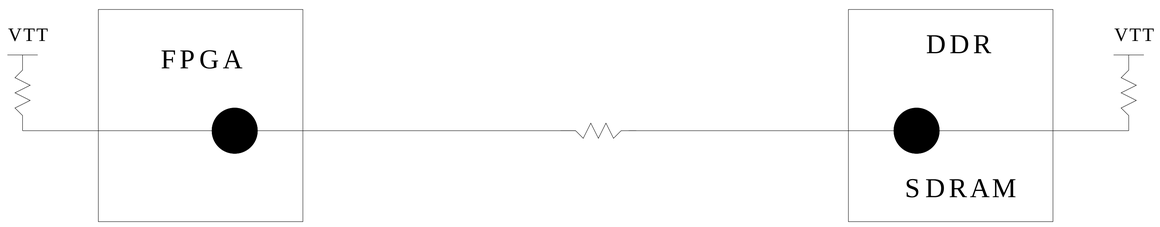
DDR_SDRAM_DATA[15:0]

DDR_SDRAM_DATA0	R637 22.1	FPGA_DDR_SDRAM_DATA0	FPGA_DDR_SDRAM_DATA[15:0]
DDR_SDRAM_DATA1	R636 22.1	FPGA_DDR_SDRAM_DATA1	
DDR_SDRAM_DATA2	R635 22.1	FPGA_DDR_SDRAM_DATA2	
DDR_SDRAM_DATA3	R634 22.1	FPGA_DDR_SDRAM_DATA3	
DDR_SDRAM_DATA4	R630 22.1	FPGA_DDR_SDRAM_DATA4	
DDR_SDRAM_DATA5	R631 22.1	FPGA_DDR_SDRAM_DATA5	
DDR_SDRAM_DATA6	R632 22.1	FPGA_DDR_SDRAM_DATA6	
DDR_SDRAM_DATA7	R633 22.1	FPGA_DDR_SDRAM_DATA7	
DDR_SDRAM_DATA8	R629 22.1	FPGA_DDR_SDRAM_DATA8	
DDR_SDRAM_DATA9	R628 22.1	FPGA_DDR_SDRAM_DATA9	
DDR_SDRAM_DATA10	R627 22.1	FPGA_DDR_SDRAM_DATA10	
DDR_SDRAM_DATA11	R626 22.1	FPGA_DDR_SDRAM_DATA11	
DDR_SDRAM_DATA12	R625 22.1	FPGA_DDR_SDRAM_DATA12	
DDR_SDRAM_DATA13	R624 22.1	FPGA_DDR_SDRAM_DATA13	
DDR_SDRAM_DATA14	R623 22.1	FPGA_DDR_SDRAM_DATA14	
DDR_SDRAM_DATA15	R622 22.1	FPGA_DDR_SDRAM_DATA15	
DDR_SDRAM_LDQS	R638 22.1	FPGA_DDR_SDRAM_LDQS	
DDR_SDRAM_UDQS	R639 22.1	FPGA_DDR_SDRAM_UDQS	

Data/DQS Termination Placement:

Place parallel terminations just beyond the SDRAM and FPGA.

Place the series terminations in between the Spartan 3A FPGA and SDRAM



VLSI Computation LAB

Title:	DDR SDRAM DATA TERMINATIONS		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: D	Sheet 19 of 43	REV: 001

Digital Temperature Sensors

*** INPUTS ***

Temp Sensor Col. 1

15-D3,15-D5,20-E2 — FPGA_TMPSENS_1A_SCK
15-D3,15-D5,20-E2 — FPGA_TMPSENS_1A_CSN
15-D3,15-D5,20-E2 — FPGA_TMPSENS_1A_MOSI
15-B1,15-D5,20-E2 — FPGA_TMPSENS_1B_SCK
15-B1,15-D5,20-E2 — FPGA_TMPSENS_1B_CSN
15-B1,15-D5,20-E2 — FPGA_TMPSENS_1B_MOSI
15-C3,15-D5,20-E2 — FPGA_TMPSENS_1C_SCK
14-D4,14-E5,20-E2 — FPGA_TMPSENS_1C_CSN
15-B3,15-D5,20-E2 — FPGA_TMPSENS_1C_MOSI

Temp Sensor Col. 2

15-C3,15-C5,20-D2 — FPGA_TMPSENS_2A_SCK
15-C5,15-D3,20-D2 — FPGA_TMPSENS_2A_CSN
15-C5,15-D3,20-D2 — FPGA_TMPSENS_2A_MOSI
15-C3,15-C5,20-D2 — FPGA_TMPSENS_2B_SCK
15-C3,15-C5,20-D2 — FPGA_TMPSENS_2B_CSN
15-C3,15-C5,20-D2 — FPGA_TMPSENS_2B_MOSI
15-C5,15-D1,20-D2 — FPGA_TMPSENS_2C_SCK
15-C5,15-D1,20-D2 — FPGA_TMPSENS_2C_CSN
15-C5,15-D1,20-D2 — FPGA_TMPSENS_2C_MOSI

*** OUTPUTS ***

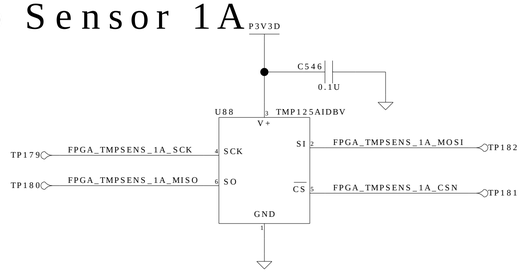
Temp Sensor Col. 1

FPGA_TMPSENS_1A_MISO — 15-D1,15-D3,20-E7
FPGA_TMPSENS_1B_MISO — 15-B1,15-D1,20-E7
FPGA_TMPSENS_1C_MISO — 15-B3,15-D1,20-E7

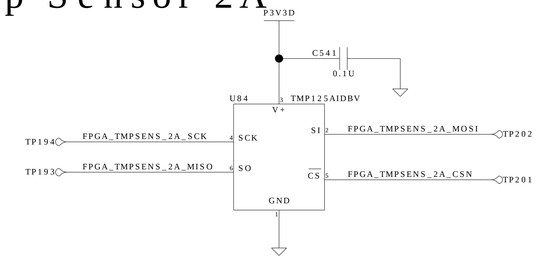
Temp Sensor Col. 2

FPGA_TMPSENS_2A_MISO — 15-D1,15-D3,20-E7
FPGA_TMPSENS_2B_MISO — 15-C3,15-D1,20-E7
FPGA_TMPSENS_2C_MISO — 15-D1,20-E7

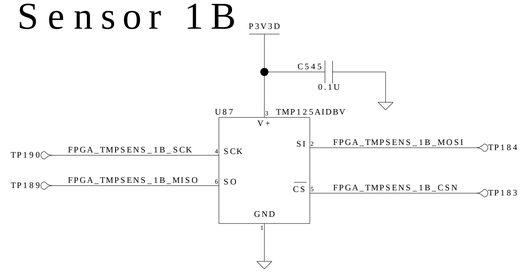
A Temp Sensor 1A



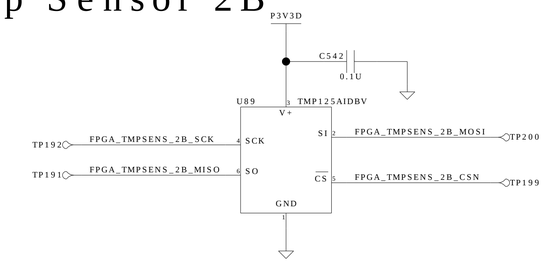
D Temp Sensor 2A



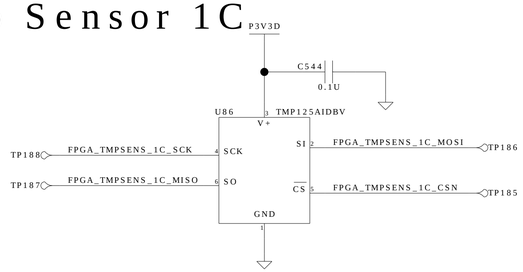
B Temp Sensor 1B



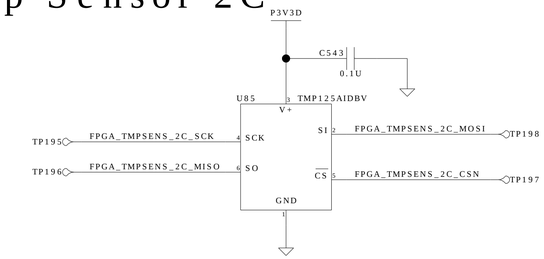
E Temp Sensor 2B

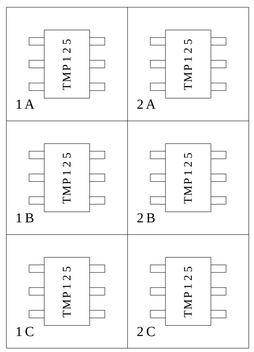


C Temp Sensor 1C



F Temp Sensor 2C



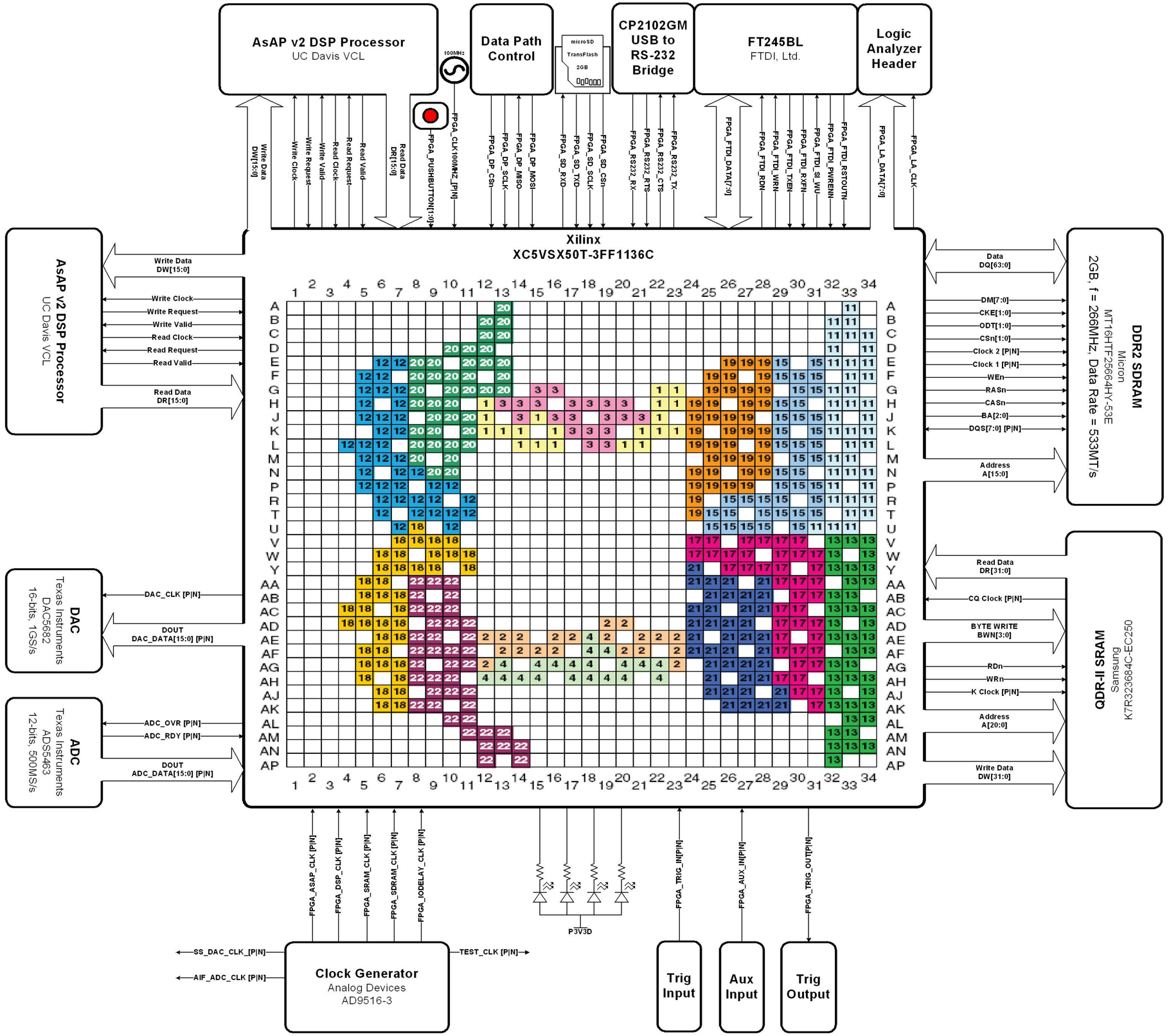


Temp sensors will be placed on a 2x3 Grid on the bottom side of the Clock Path board.

VLSI Computation LAB

Title:	DIGITAL TEMPERATURE SENSORS		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: D	Sheet 20 of 43 REV: 001

Data Path FPGA Digital Design



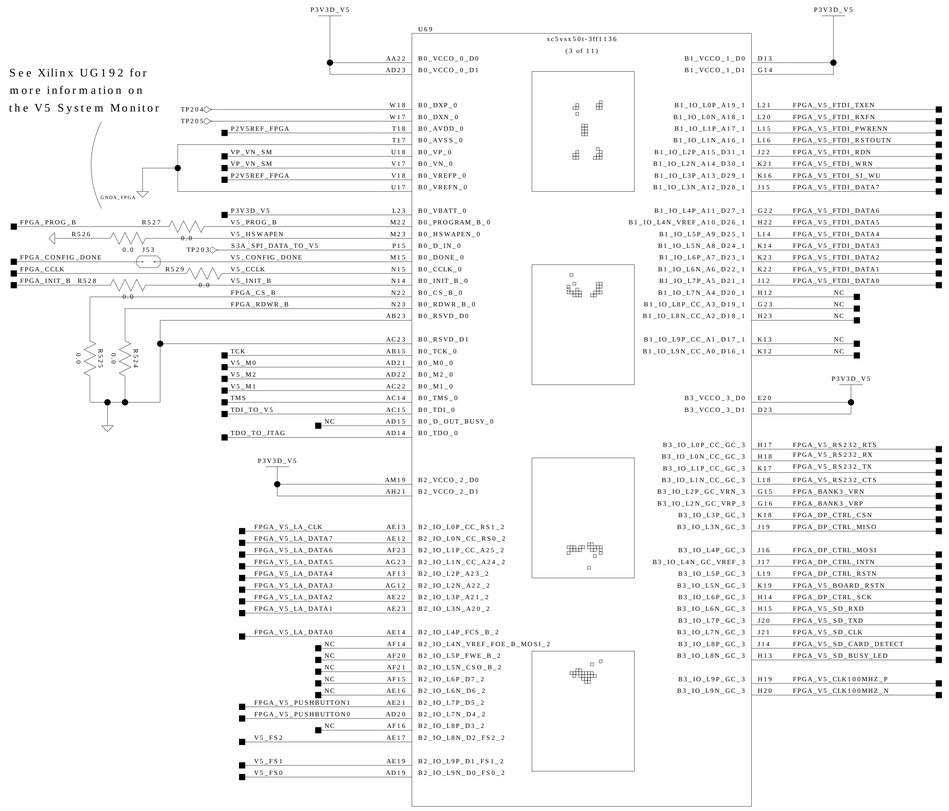
VLSI Computation LAB

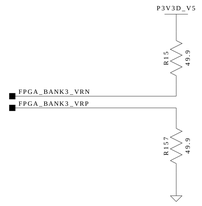
Title:	DATA PATH FPGA DIGITAL DESIGN		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 21 of 43	REV: 001

Xilinx Virtex-5 SX50T Configuration

Spartan 3A: VCCO_2 = 3.3V, VCCAUX = 3.3V
Virtex 5 SX50T: VCCO_0 = 3.3V, VCCO_2 = 3.3V

See Xilinx UG192 for more information on the V5 System Monitor





** INPUTS **

SPI Configuration

14-D4,22-E1 → S3A_SPI_DATA_TO_V5
14-D3,22-D1,22-E1 → FPGA_PROG_B
14-B3,14-C4,14-D3,22-D1 22-E1 → FPGA_CCLK

JTAG Configuration

14-D4,22-D2,22-E1 → TDI_TO_V5
14-C3,14-D4,22-D2,22-E1 → TMS
14-C3,14-D4,22-D2,22-E1 → TCK

LVPECL Clocks

12-B3,12-E5,22-E1,22-E3 → FPGA_ASAP_CLKIN_P
12-B3,12-E5,22-E1,22-E3 → FPGA_ASAP_CLKIN_N
12-A3,12-E5,22-E1,22-E3 → FPGA_DSP_CLKIN_P
12-A3,12-E5,22-E1,22-E3 → FPGA_DSP_CLKIN_N

LVDS Clocks

12-C3,12-E5,22-E1,22-E3 → FPGA_SRAM_CLK_P
12-C3,12-E5,22-E1,22-E3 → FPGA_SRAM_CLK_N
12-C3,12-E5,22-E1,22-E3 → FPGA_SDRAM_CLK_P
12-C3,12-E5,22-E1,22-E3 → FPGA_SDRAM_CLK_N
12-C3,12-E5,22-D1,22-E1 → FPGA_IODELAY_CLK_P
12-C3,12-E5,22-D1,22-D3 → FPGA_IODELAY_CLK_N

Data Path FPGA Control

15-B5,15-C3,22-D1,22-D3 → FPGA_DP_CTRL_MOSI
15-B3,15-B5,22-D1,22-D3 → FPGA_DP_CTRL_CSN
15-B3,15-B5,22-D1,22-D3 → FPGA_DP_CTRL_SCK
15-B3,15-B5,22-D1,22-D3 → FPGA_DP_CTRL_RSTN

USB to RS-232 Interface

22-D1,22-D3,30-E5 → FPGA_V5_RS232_RTS
22-D1,22-D3,30-E5 → FPGA_V5_RS232_RX

Debug LEDs

22-D1,22-D3,30-C2,30-E5 → FPGA_V5_LEDS[3:0]

Debug Push Buttons

22-C2,22-D1,30-C2,30-E5 → FPGA_V5_PUSHBUTTON[1:0]

MicroSD Interface

22-C3,22-D1,30-E5 → FPGA_V5_SD_RXD

100MHz FPGA Clock

22-C3,22-D1,30-B3,30-E5 → FPGA_V5_CLK100MHZ_P
22-C3,22-D1,30-B3,30-D5 → FPGA_V5_CLK100MHZ_N

Auxiliary Input

22-D1,22-D3,35-B3,35-E5 → FPGA_AUX_IN_P
22-D1,22-D3,35-B3,35-E5 → FPGA_AUX_IN_N

Trigger Input

22-C1,22-D3,35-D3,35-E5 → FPGA_TRIG_IN_P
22-C1,22-D3,35-D3,35-E5 → FPGA_TRIG_IN_N

FT245BL USB Interface

22-C1,22-D3,22-E3,30-C5 → FPGA_V5_FTDI_DATA[7:0]
22-C1,22-E3,30-C4,30-D5 → FPGA_V5_FTDI_TXEN
22-C1,22-E3,30-C4,30-D5 → FPGA_V5_FTDI_RXFN
22-C1,22-E3,30-C4,30-D5 → FPGA_V5_FTDI_PWRENN
22-C1,22-E3,30-D5 → FPGA_V5_FTDI_RSTOUTN

Custom Configuration

15-E5,22-C1 → V5_PROG_B
15-E5,22-C1 → V5_CCLK

Board Reset

17-B3,17-E5,22-C1,22-D3 → FPGA_V5_BOARD_RSTN

** OUTPUTS **

SPI Configuration

FPGA_CONFIG_DONE → 17-B1,22-D1,22-E5
FPGA_INIT_B → 22-D1,22-E5

JTAG Configuration

TDO_TO_JTAG → 14-C3,22-D2,22-E5

Data Path FPGA Control

FPGA_DP_CTRL_MISO → 15-B3,15-C1,22-D3,22-E5
FPGA_DP_CTRL_INTN → 15-B3,15-C1,22-D3,22-E5

MicroSD Interface

FPGA_V5_SD_TXD → 22-C3,22-E5,30-E1
FPGA_V5_SD_CLK → 22-C3,22-E5,30-E1
FPGA_V5_SD_CARD_DETECT → 22-C3,22-E5,30-E1
FPGA_V5_SD_BUSY_LED → 22-C3,22-E5,30-B4,30-E1

USB to RS-232

FPGA_V5_RS232_TX → 22-D3,22-E5,30-E1
FPGA_V5_RS232_CTS → 22-D3,22-E5,30-E1

Trigger Output

FPGA_TRIG_OUT_P → 22-D3,22-D5,35-D3,35-E1
FPGA_TRIG_OUT_N → 22-D3,22-D5,35-D3,35-E1

FT245BL USB Interface

FPGA_V5_FTDI_RDN → 22-D5,22-E3,30-C4,30-E1
FPGA_V5_FTDI_WRN → 22-D5,22-E3,30-C4,30-E1
FPGA_V5_FTDI_SI_WU → 22-D5,22-E3,30-C4,30-E1

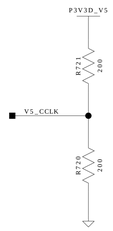
Custom Configuration

V5_INIT_B → 15-B1,22-D5
V5_CONFIG_DONE → 15-B1,22-D5

Logic Analyzer

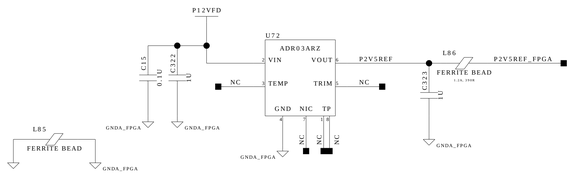
FPGA_V5_LA_CLK → 22-D2,22-D5,30-B5,30-E1
FPGA_V5_LA_DATA[7:0] → 22-C2,22-D2,22-D5,30-B5 30-E1

B Virtex-5 SX50T CCLK



NOTES:
FPGA_CCLK requires an end termination and is a 50 Ohm controlled impedance transmission line. The end termination must be placed near the Configuration PROM.
FPGA_CCLK Stub Length from S3A to SPI Flash < 12.5 mm

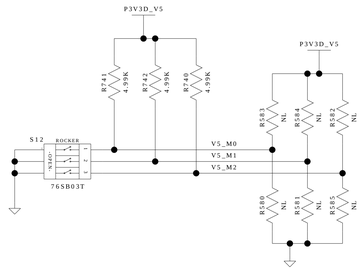
C System Monitor Precision Reference



See pages 46-49 of Xilinx UG192 for PC Design Guidlines

D Virtex-5 SX50T FPGA Configuration Mode

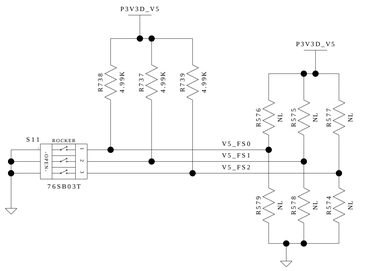
CONFIG MODE	M2	M1	M0	DATA WIDTH	CCLK Direction
Master Serial	0	0	0	1 bit	Output
Master SPI	0	0	1	1 bit	Output
Master BPI-Up	0	1	0	8, 16 bits	Output
Master BPI-Down	0	1	1	8, 16 bits	Output
"Master SelectMAP"	1	0	0	8, 16 bits	Output
JTAG/Bndry Scan	1	0	1	1 bit	Input (TCK)
Slave SelectMAP	1	1	0	8, 16, 32 bits	Input
Slave Serial	1	1	1	1 bit	Input



For more information see Xilinx Virtex 5 Configuration Guide (UG191)

E Virtex-5 SX50T FPGA SPI Mode

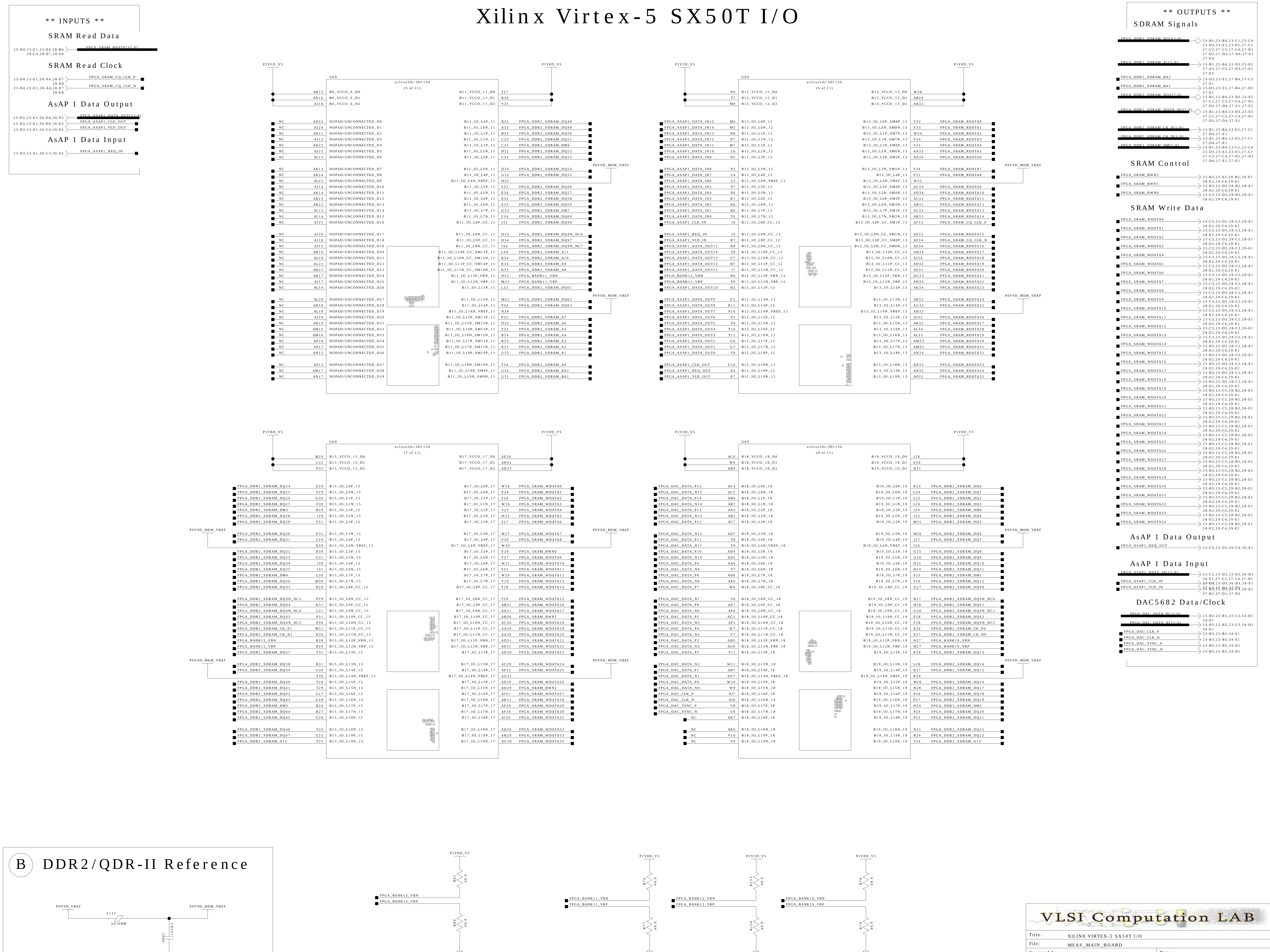
FS2	FS1	FS0	HEX CMD CODE
0	0	0	0xFF
0	0	1	RCMD[7:0]
0	1	0	0x52
0	1	1	RESERVED
1	0	0	0x55
1	0	1	0x03
1	1	0	0xE8
1	1	1	0x0B



VLSI Computation LAB

Title:	XILINX VIRTEX-5 SX50T CONFIGURATION		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 22 of 43	REV: 001

Xilinx Virtex-5 SX50T I/O



VLSI Computation LAB

Title:	XILINX VIRTEX-5 SX50T I/O		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 23 of 43	REV: 001

Xilinx Virtex-5 SX50T I/O

** INPUTS **

AsAP 2 Data Output

24-C2,24-D2,24-E1,40-D4 40-E5 — FPGA_ASAP2_DATA_OUT[15:0]

24-C2,24-E1,40-D4,40-E5 — FPGA_ASAP2_CLK_OUT

24-C2,24-E1,40-C4,40-E5 — FPGA_ASAP2_VLD_OUT

AsAP 2 Data Input

24-D2,24-E1,40-D3,40-E5 — FPGA_ASAP2_REQ_IN

ADS5463 Data/Clock

24-C3,24-D3,24-E1,33-B5 33-C5 — FPGA_ADC_DATA_P[15:0]

24-C3,24-D3,24-E1,33-B5 33-C5 — FPGA_ADC_DATA_N[15:0]

24-C3,24-E1,33-C5 — FPGA_ADC_OVR_P

24-C3,24-E1,33-C5 — FPGA_ADC_OVR_N

24-C3,24-E1,33-C5 — FPGA_ADC_DATA_RDY_P

24-C3,24-E1,33-C5 — FPGA_ADC_DATA_RDY_N

** OUTPUTS **

AsAP 2 Data Output

FPGA_ASAP2_REQ_OUT → 24-C2,24-E5,40-D4,40-E1

AsAP 2 Data Input

FPGA_ASAP2_DATA_IN[15:0] → 24-D2,24-E5,40-D3,40-E1 41-C2,41-C4,41-E1,41-E2

FPGA_ASAP2_CLK_IN → 24-D2,24-E5,40-D3,40-E1 41-C2,41-C4,41-E1,41-E2

FPGA_ASAP2_VLD_IN → 24-D2,24-E5,40-D3,40-E1 41-C2,41-D1,41-D2

SRAM Control

FPGA_SRAM_WRN → 24-C3,24-E5,28-B2,28-E1 28-E2,29-C4,29-E1

FPGA_SRAM_RDN → 24-C3,24-E5,28-B4,28-E1 28-E2,29-C4,29-E1

FPGA_SRAM_WDATA35 → 24-D3,24-E5,28-B2,28-E1 28-E2,29-C4,29-E1

FPGA_SRAM_BWN3 → 24-D3,24-E5,28-A2,28-E1 28-E2,29-C4,29-E1

FPGA_SRAM_ADDR[17:0] → 24-C3,24-D3,24-E5,28-C7 28-E1,28-E2,29-C3,29-E1

SRAM Clocks

FPGA_SRAM_K_CLK_P → 24-D3,24-E5,28-A2,28-D1 28-D2,29-B3,29-E1

FPGA_SRAM_K_CLK_N → 24-D3,24-E5,28-A2,28-D1 28-D2,29-B3,29-E1

FPGA_SRAM_C_CLK_P → 24-D3,24-D5,28-D1,28-D2 29-B4,29-D1

FPGA_SRAM_C_CLK_N → 24-D3,24-D5,28-D1,28-D2 29-B4,29-D1

SDRAM Signals

FPGA_DDR2_SDRAM_RASN → 24-C3,24-D5,27-A5,27-D3 27-E1

FPGA_DDR2_SDRAM_CASN → 24-C3,24-D5,27-A5,27-D3 27-E1

FPGA_DDR2_SDRAM_WEN → 24-C3,24-D5,27-A5,27-D3 27-E1

FPGA_DDR2_SDRAM_CKE[1:0] → 24-C3,24-D5,27-A4,27-C2 27-E1

FPGA_DDR2_SDRAM_SN[1:0] → 24-C3,24-D5,27-A4,27-D1 27-D3

FPGA_DDR2_SDRAM_ODT[1:0] → 24-C3,24-D5,27-A4,27-D1 27-D3

FPGA_DDR2_SDRAM_BA0 → 24-C3,24-D5,27-B4,27-D3 27-E1

P2V5D_V5 P1V8D_V5

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	J8	B20_VCCO_20_D0	B21_VCCO_21_D0	AJ28	
	E10	B20_VCCO_20_D1	B21_VCCO_21_D1	AM29	
	H11	B20_VCCO_20_D2	B21_VCCO_21_D2	AL32	
FPGA_ASAP2_DATA_IN15	E9	B20_IO_L0P_20	B21_IO_L0P_21	AA25	FPGA_SRAM_K_CLK_P
FPGA_ASAP2_DATA_IN14	E8	B20_IO_L0N_20	B21_IO_L0N_21	AA26	FPGA_SRAM_K_CLK_N
FPGA_ASAP2_DATA_IN13	F9	B20_IO_L1P_20	B21_IO_L1P_21	AB27	FPGA_SRAM_C_CLK_P
FPGA_ASAP2_DATA_IN12	F8	B20_IO_L1N_20	B21_IO_L1N_21	AC27	FPGA_SRAM_C_CLK_N
FPGA_ASAP2_DATA_IN11	F10	B20_IO_L2P_20	B21_IO_L2P_21	Y24	FPGA_SRAM_WDATA35
FPGA_ASAP2_DATA_IN10	G10	B20_IO_L2N_20	B21_IO_L2N_21	AA24	FPGA_SRAM_BWN3
FPGA_ASAP2_DATA_IN9	G8	B20_IO_L3P_20	B21_IO_L3P_21	AB25	FPGA_SRAM_ADDR17
FPGA_ASAP2_DATA_IN8	H8	B20_IO_L3N_20	B21_IO_L3N_21	AB26	FPGA_SRAM_ADDR16
FPGA_ASAP2_DATA_IN7	D11	B20_IO_L4P_20	B21_IO_L4P_21	AC28	FPGA_SRAM_ADDR15
FPGA_ASAP2_DATA_IN6	D10	B20_IO_L4N_VREF_20	B21_IO_L4N_VREF_21	AD27	
FPGA_ASAP2_DATA_IN5	K11	B20_IO_L5P_20	B21_IO_L5P_21	AB28	FPGA_SRAM_ADDR14
FPGA_ASAP2_DATA_IN4	J11	B20_IO_L5N_20	B21_IO_L5N_21	AA28	FPGA_SRAM_ADDR13
FPGA_ASAP2_DATA_IN3	D12	B20_IO_L6P_20	B21_IO_L6P_21	AG28	FPGA_SRAM_ADDR12
FPGA_ASAP2_DATA_IN2	C12	B20_IO_L6N_20	B21_IO_L6N_21	AH28	FPGA_SRAM_ADDR11
FPGA_ASAP2_DATA_IN1	H10	B20_IO_L7P_20	B21_IO_L7P_21	AE28	FPGA_SRAM_ADDR10
FPGA_ASAP2_DATA_IN0	H9	B20_IO_L7N_20	B21_IO_L7N_21	AF28	FPGA_SRAM_ADDR9
FPGA_ASAP2_CLK_IN	A13	B20_IO_L8P_CC_20	B21_IO_L8P_CC_21	AK26	FPGA_SRAM_ADDR8
FPGA_ASAP2_REQ_IN	B12	B20_IO_L8N_CC_20	B21_IO_L8N_CC_21	AJ27	FPGA_SRAM_ADDR7
FPGA_ASAP2_VLD_IN	J10	B20_IO_L9P_CC_20	B21_IO_L9P_CC_21	AK29	FPGA_SRAM_ADDR6
FPGA_ASAP2_DATA_OUT15	J9	B20_IO_L9N_CC_20	B21_IO_L9N_CC_21	AJ29	FPGA_SRAM_ADDR5
FPGA_ASAP2_DATA_OUT14	K8	B20_IO_L10P_CC_20	B21_IO_L10P_CC_21	AK28	FPGA_SRAM_ADDR4
FPGA_ASAP2_DATA_OUT13	K9	B20_IO_L10N_CC_20	B21_IO_L10N_CC_21	AK27	FPGA_SRAM_ADDR3
FPGA_ASAP2_DATA_OUT12	B13	B20_IO_L11P_CC_20	B21_IO_L11P_CC_21	AH27	FPGA_SRAM_ADDR2
FPGA_ASAP2_DATA_OUT11	C13	B20_IO_L11N_CC_20	B21_IO_L11N_CC_21	AJ26	FPGA_SRAM_ADDR1
FPGA_BANK20_VRN	L10	B20_IO_L12P_VRN_20	B21_IO_L12P_VRN_21	AJ25	FPGA_BANK21_VRN
FPGA_BANK20_VRP	L11	B20_IO_L12N_VRP_20	B21_IO_L12N_VRP_21	AH25	FPGA_BANK21_VRP
FPGA_ASAP2_DATA_OUT10	G11	B20_IO_L13P_20	B21_IO_L13P_21	AF24	FPGA_SRAM_ADDR0
FPGA_ASAP2_DATA_OUT9	G12	B20_IO_L13N_20	B21_IO_L13N_21	AG25	FPGA_SRAM_WRN
FPGA_ASAP2_DATA_OUT8	M8	B20_IO_L14P_20	B21_IO_L14P_21	AG27	FPGA_SRAM_RDN
FPGA_ASAP2_DATA_OUT7	L8	B20_IO_L14N_VREF_20	B21_IO_L14N_VREF_21	AG26	
FPGA_ASAP2_DATA_OUT6	F11	B20_IO_L15P_20	B21_IO_L15P_21	AF25	FPGA_DDR2_SDRAM_BA0
FPGA_ASAP2_DATA_OUT5	E11	B20_IO_L15N_20	B21_IO_L15N_21	AF26	FPGA_DDR2_SDRAM_RASN
FPGA_ASAP2_DATA_OUT4	M10	B20_IO_L16P_20	B21_IO_L16P_21	AE27	FPGA_DDR2_SDRAM_CASN
FPGA_ASAP2_DATA_OUT3	L9	B20_IO_L16N_20	B21_IO_L16N_21	AE26	FPGA_DDR2_SDRAM_WEN
FPGA_ASAP2_DATA_OUT2	E12	B20_IO_L17P_20	B21_IO_L17P_21	AC25	FPGA_DDR2_SDRAM_SN1
FPGA_ASAP2_DATA_OUT1	E13	B20_IO_L17N_20	B21_IO_L17N_21	AC24	FPGA_DDR2_SDRAM_SN0
FPGA_ASAP2_DATA_OUT0	N10	B20_IO_L18P_20	B21_IO_L18P_21	AD26	FPGA_DDR2_SDRAM_ODT1
FPGA_ASAP2_CLK_OUT	N9	B20_IO_L18N_20	B21_IO_L18N_21	AD25	FPGA_DDR2_SDRAM_ODT0
FPGA_ASAP2_REQ_OUT	F13	B20_IO_L19P_20	B21_IO_L19P_21	AD24	FPGA_DDR2_SDRAM_CKE1
FPGA_ASAP2_VLD_OUT	G13	B20_IO_L19N_20	B21_IO_L19N_21	AE24	FPGA_DDR2_SDRAM_CKE0

P0V9D_MEM_VREF

P0V9D_MEM_VREF

P2V5D_V5 P1V8D_V5

R155 49.9 — FPGA_BANK20_VRN

R156 49.9 — FPGA_BANK20_VRP

R83 49.9 — FPGA_BANK21_VRN

R82 49.9 — FPGA_BANK21_VRP

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	AF7	B22_VCCO_22_D0	B23_VCCO_23_D0	G24	
	AJ8	B22_VCCO_22_D1	B23_VCCO_23_D1	C26	
	AH11	B22_VCCO_22_D2	B23_VCCO_23_D2	F27	
FPGA_ADC_DATA_P15	AN14	B22_IO_L0P_22	NOPAD/UNCONNECTED_D0	C20	NC
FPGA_ADC_DATA_N15	AP14	B22_IO_L0N_22	NOPAD/UNCONNECTED_D1	B20	NC
FPGA_ADC_DATA_P14	AB10	B22_IO_L1P_22	NOPAD/UNCONNECTED_D2	B21	NC
FPGA_ADC_DATA_N14	AA10	B22_IO_L1N_22	NOPAD/UNCONNECTED_D3	A21	NC
FPGA_ADC_DATA_P13	AN13	B22_IO_L2P_22	NOPAD/UNCONNECTED_D4	C19	NC
FPGA_ADC_DATA_N13	AM13	B22_IO_L2N_22	NOPAD/UNCONNECTED_D5	C18	NC
FPGA_ADC_DATA_P12	AA8	B22_IO_L3P_22	NOPAD/UNCONNECTED_D6	C22	NC
FPGA_ADC_DATA_N12	AA9	B22_IO_L3N_22	NOPAD/UNCONNECTED_D7	B22	NC
FPGA_ADC_DATA_P11	AP12	B22_IO_L4P_22	NOPAD/UNCONNECTED_D8	B18	NC
FPGA_ADC_DATA_N11	AN12	B22_IO_L4N_VREF_22	NOPAD/UNCONNECTED_D9	A18	NC
FPGA_ADC_DATA_P10	AC8	B22_IO_L5P_22	NOPAD/UNCONNECTED_D10	C23	NC
FPGA_ADC_DATA_N10	AB8	B22_IO_L5N_22	NOPAD/UNCONNECTED_D11	B23	NC
FPGA_ADC_DATA_P9	AM12	B22_IO_L6P_22	NOPAD/UNCONNECTED_D12	A19	NC
FPGA_ADC_DATA_N9	AM11	B22_IO_L6N_22	NOPAD/UNCONNECTED_D13	A20	NC
FPGA_ADC_DATA_P8	AC10	B22_IO_L7P_22	NOPAD/UNCONNECTED_D14	A23	NC
FPGA_ADC_DATA_N8	AC9	B22_IO_L7N_22	NOPAD/UNCONNECTED_D15	A24	NC
FPGA_ADC_DATA_P7	AL11	B22_IO_L8P_CC_22	NOPAD/UNCONNECTED_D16	C24	NC
FPGA_ADC_DATA_N7	AL10	B22_IO_L8N_CC_22	NOPAD/UNCONNECTED_D17	D25	NC
FPGA_ADC_DATA_P6	AE8	B22_IO_L9P_CC_22	NOPAD/UNCONNECTED_D18	B26	NC
FPGA_ADC_DATA_N6	AD9	B22_IO_L9N_CC_22	NOPAD/UNCONNECTED_D19	A25	NC
FPGA_ADC_DATA_P5	AD10	B22_IO_L10P_CC_22	NOPAD/UNCONNECTED_D20	B27	NC
FPGA_ADC_DATA_N5	AD11	B22_IO_L10N_CC_22	NOPAD/UNCONNECTED_D21	A26	NC
FPGA_ADC_DATA_P4	AK11	B22_IO_L11P_CC_22	NOPAD/UNCONNECTED_D22	B25	NC
FPGA_ADC_DATA_N4	AJ11	B22_IO_L11N_CC_22	NOPAD/UNCONNECTED_D23	C25	NC
FPGA_ADC_DATA_P3	AF8	B22_IO_L12P_VRN_22	NOPAD/UNCONNECTED_D24	C29	NC
FPGA_ADC_DATA_N3	AE9	B22_IO_L12N_VRP_22	NOPAD/UNCONNECTED_D25	B28	NC
FPGA_ADC_DATA_P2	AK8	B22_IO_L13P_22	NOPAD/UNCONNECTED_D26	D26	NC
FPGA_ADC_DATA_N2	AK9	B22_IO_L13N_22	NOPAD/UNCONNECTED_D27	C27	NC
FPGA_ADC_DATA_P1	AF9	B22_IO_L14P_22	NOPAD/UNCONNECTED_D28	A27	NC
FPGA_ADC_DATA_N1	AF10	B22_IO_L14N_VREF_22	NOPAD/UNCONNECTED_D29	A28	NC
FPGA_ADC_DATA_P0	AJ9	B22_IO_L15P_22	NOPAD/UNCONNECTED_D30	C28	NC
FPGA_ADC_DATA_N0	AJ10	B22_IO_L15N_22	NOPAD/UNCONNECTED_D31	D27	NC
FPGA_ADC_OVR_P	AF11	B22_IO_L16P_22	NOPAD/UNCONNECTED_D32	B31	NC
FPGA_ADC_OVR_N	AE11	B22_IO_L16N_22	NOPAD/UNCONNECTED_D33	A31	NC
FPGA_ADC_DATA_RDY_P	AH9	B22_IO_L17P_22	NOPAD/UNCONNECTED_D34	C30	NC
FPGA_ADC_DATA_RDY_N	AH10	B22_IO_L17N_22	NOPAD/UNCONNECTED_D35	D29	NC
NC	AG8	B22_IO_L18P_22	NOPAD/UNCONNECTED_D36	B31	NC
NC	AH8	B22_IO_L18N_22	NOPAD/UNCONNECTED_D37	D30	NC
NC	AG10	B22_IO_L19P_22	NOPAD/UNCONNECTED_D38	A30	NC
NC	AG11	B22_IO_L19N_22	NOPAD/UNCONNECTED_D39	B30	NC

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	AL22	B25_VCCO_25_D0			
	AK25	B25_VCCO_25_D1			
	AN26	B25_VCCO_25_D2			
NC	AL29	NOPAD/UNCONNECTED_D0			
NC	AL30	NOPAD/UNCONNECTED_D1			
NC	AM31	NOPAD/UNCONNECTED_D2			
NC	AL31	NOPAD/UNCONNECTED_D3			
NC	AN30	NOPAD/UNCONNECTED_D4			
NC	AM30	NOPAD/UNCONNECTED_D5			
NC	AP30	NOPAD/UNCONNECTED_D6			
NC	AP31	NOPAD/UNCONNECTED_D7			
NC	AM27	NOPAD/UNCONNECTED_D8			
NC	AL28	NOPAD/UNCONNECTED_D9			
NC	AP29	NOPAD/UNCONNECTED_D10			
NC	AN29	NOPAD/UNCONNECTED_D11			
NC	AP27	NOPAD/UNCONNECTED_D12			
NC	AN27	NOPAD/UNCONNECTED_D13			
NC	AN28	NOPAD/UNCONNECTED_D14			
NC	AM28	NOPAD/UNCONNECTED_D15			
NC	AN25	NOPAD/UNCONNECTED_D16			
NC	AM25	NOPAD/UNCONNECTED_D17			
NC	AM26	NOPAD/UNCONNECTED_D18			
NC	AL26	NOPAD/UNCONNECTED_D19			
NC	AP26	NOPAD/UNCONNECTED_D20			
NC	AP25	NOPAD/UNCONNECTED_D21			
NC	AL25	NOPAD/UNCONNECTED_D22			
NC	AL24	NOPAD/UNCONNECTED_D23			
NC	AN24	NOPAD/UNCONNECTED_D24			
NC	AP24	NOPAD/UNCONNECTED_D25			
NC	AM21	NOPAD/UNCONNECTED_D26			
NC	AM20	NOPAD/UNCONNECTED_D27			
NC	AN23	NOPAD/UNCONNECTED_D28			
NC	AM23	NOPAD/UNCONNECTED_D29			
NC	AN20	NOPAD/UNCONNECTED_D30			
NC	AP20	NOPAD/UNCONNECTED_D31			
NC	AN22	NOPAD/UNCONNECTED_D32			
NC	AM22	NOPAD/UNCONNECTED_D33			
NC	AN18	NOPAD/UNCONNECTED_D34			
NC	AM18	NOPAD/UNCONNECTED_D35			
NC	AP22	NOPAD/UNCONNECTED_D36			
NC	AP21	NOPAD/UNCONNECTED_D37			
NC	AN19	NOPAD/UNCONNECTED_D38			
NC	AP19	NOPAD/UNCONNECTED_D39			

VLSI Computation LAB

Title:	XILINX VIRTEX-5 SX50T I/O		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 24 of 43	REV: 001

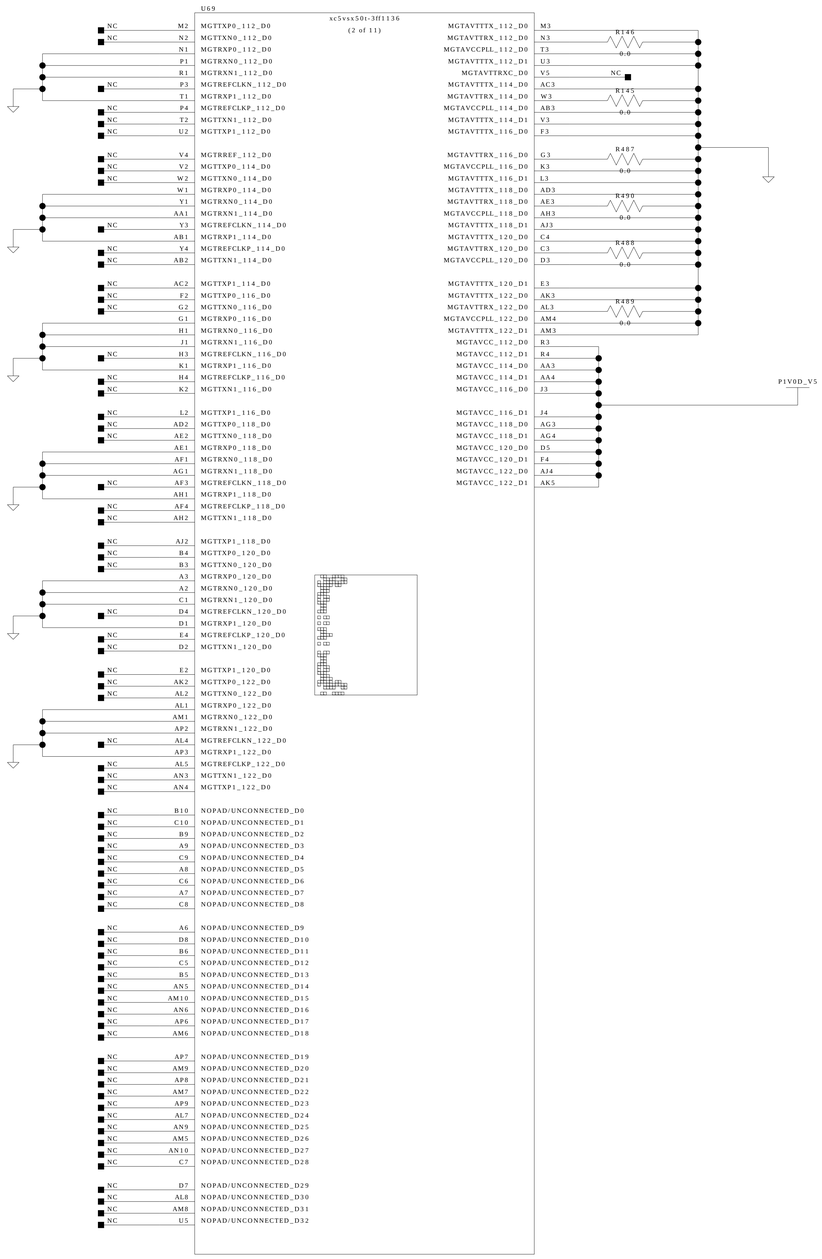
Xilinx Virtex-5 SX50T MGT I/O and Power Inputs

Table 10-5: **GTP_DUAL Power Supply Connections for a Completely Unused GTP_DUAL Column**

Pin or Pin Pair	Connect To
MGTRXP/MGTRXN	GND
MGTTXP/MGTTXN	Floating, No connection
MGTREFCLKP/MGTREFCLKN	Floating, No connection
MGTTTX	GND
MGTTRX	GND
MGTAVTTRXC	Floating, No connection
MGTAVCCPLL	GND
MGTAVCC(1)	V_{CCINT} or GND

Notes:

1. If Boundary-Scan is part of the product verification, connect the analog supply voltage pin MGTAVCC of all GTP_DUAL tiles directly without filtering to the V_{CCINT} pins of the device. If Boundary-Scan is *not* part of the product verification, connect MGTAVCC to GND.



VLSI Computation LAB

Title:	XILINX VIRTEX-5 SX50T MGT I/O AND POWER INPUTS		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 25 of 43	REV: 001

Xilinx Virtex-5 SX50T Core, I/O, and Auxiliary Power Inputs

P2V5D

L27 42-OHM

Rated @ 6A

P2V5D_V5

+C396 47U · +C364 47U · +C365 47U · +C366 47U · +C367 47U · +C368 47U · +C369 47U · +C431 33U · C280 0.22U · C279 0.22U · C278 0.22U · C277 0.22U · C276 0.22U · C283 0.22U · C282 0.22U · C281 0.22U

C690 0.1UF · C694 0.1UF · C693 0.1UF · C695 0.1UF · C692 0.1UF · C691 0.1UF · C715 0.1UF · C714 0.1UF

C713 0.1UF · C709 0.1UF · C710 0.1UF · C708 0.1UF · C711 0.1UF · C712 0.1UF · C719 0.1UF · C720 0.1UF

C702 0.1UF · C706 0.1UF · C705 0.1UF · C707 0.1UF · C704 0.1UF · C703 0.1UF · C718 0.1UF · C717 0.1UF

C701 0.1UF · C697 0.1UF · C698 0.1UF · C696 0.1UF · C699 0.1UF · C700 0.1UF · C716 0.1UF · C721 0.1UF

P1V0D

L28 42-OHM

Rated @ 6A

P1V0D_V5

C391 0.22U · C284 0.22U · C285 0.22U · C286 0.22U

C722 0.1UF · C726 0.1UF · C728 0.1UF · C727 0.1UF · C319 0.1UF · C309 0.1UF

C304 0.22U · C307 0.22U · C306 0.22U · C305 0.22U

C753 0.1UF · C752 0.1UF · C750 0.1UF · C751 0.1UF · C215 0.1UF · C214 0.1UF

C300 0.22U · C303 0.22U · C302 0.22U · C301 0.22U

C749 0.1UF · C748 0.1UF · C746 0.1UF · C747 0.1UF · C399 0.1UF · C320 0.1UF

C290 0.22U · C289 0.22U · C288 0.22U · C287 0.22U

C723 0.1UF · C729 0.1UF · C725 0.1UF · C724 0.1UF · +C157 330U · +C156 330U

P3V3D

L30 42-OHM

Rated @ 6A

P3V3D_V5

C308 0.22U · C293 0.22U · C292 0.22U · C370 47U · C371 47U

C755 0.1UF · C754 0.1UF · C733 0.1UF · C731 0.1UF · C730 0.1UF · C732 0.1UF · C472 0.1UF · C471 0.1UF

C761 0.1UF · C760 0.1UF · C756 0.1UF · C758 0.1UF · C759 0.1UF · C757 0.1UF · C469 0.1UF · C470 0.1UF

P1V8D

L31 BMB1608-42

Rated @ 6A

P1V8D_V5

C377 47U · C376 47U · C375 47U · C374 47U · C372 47U · C373 47U

C294 0.22U · C295 0.22U · C296 0.22U · C297 0.22U · C299 0.22U · C298 0.22U

C212 0.1UF · C213 0.1UF

C744 0.1UF · C742 0.1UF · C741 0.1UF · C743 0.1UF · C211 0.1UF

C745 0.1UF · C739 0.1UF · C740 0.1UF · C738 0.1UF · C210 0.1UF

C735 0.1UF · C736 0.1UF · C737 0.1UF · C734 0.1UF · C473 0.1UF

C764 0.1UF · C763 0.1UF · C762 0.1UF · C765 0.1UF · C474 0.1UF

XILINX FPGA

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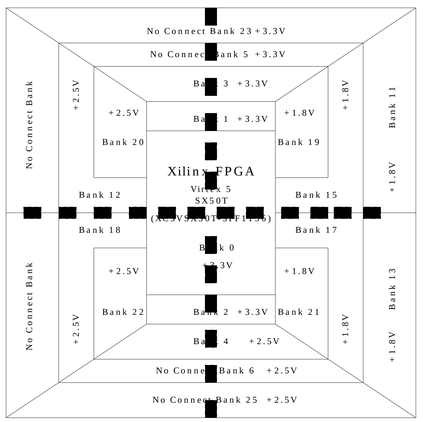
U69

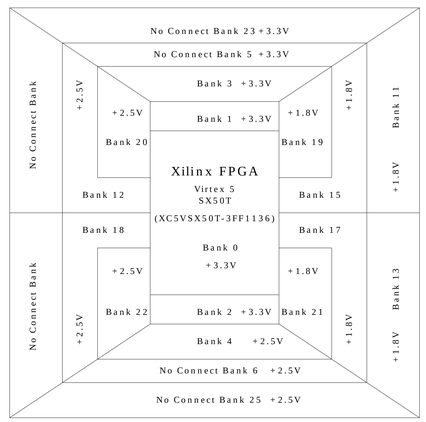
VCCAUX · VCCINT · FLOAT_D0 · NC · GND

Capacitor Placement (bottom side)

Capacitor Placement (top side)

X2Y · TANT · TANT VCCAUX





Capacitor Legend:

PWR	0402	X2Y / TANT
+1V	■	
+1.8V	■	
+2.5V	■	
+3.3V	■	

X2Y Capacitor Via Placement

Tantalum/O402 Via Placement

VLSI Computation LAB			
Title:	XILINX VIRTEX-5 SX50T CORE, I/O, AND AUXILIARY POWER INPUTS		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 26 of 43 REV: 001

DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB

256 Meg x 64-bits

Provides between 1.024 GS and 1.280 GS storage of sampled data.

** INPUTS **

SDRAM Signals

23-B1,23-B4,23-C1,23-C4
23-D3,23-E3,23-E5,27-C1
27-C2,27-C3,27-C4,27-D1
27-D2,27-D3,27-D4,27-E1
27-E4 — FPGA_DDR2_SDRAM_DQ[63:0]

23-B1,23-B4,23-D3,23-E5
27-A3,27-C2,27-D3,27-E1
27-E3 — FPGA_DDR2_SDRAM_A[15:0]

23-D3,23-E5,24-C3,24-D5
27-B4,27-C2,27-D3,27-E1 — FPGA_DDR2_SDRAM_BA[2:0]

24-C3,24-D5,27-A5,27-D3
27-E1 — FPGA_DDR2_SDRAM_RASN

24-C3,24-D5,27-A5,27-D3
27-E1 — FPGA_DDR2_SDRAM_CASN

24-C3,24-D5,27-A5,27-D3
27-E1 — FPGA_DDR2_SDRAM_WEN

24-C3,24-D5,27-A4,27-C2
27-E1 — FPGA_DDR2_SDRAM_CKE[1:0]

23-B1,23-B4,23-D3,23-E5
27-C1,27-C3,27-C4,27-D1
27-D2,27-D4,27-E1,27-E2 — FPGA_DDR2_SDRAM_DQS[7:0]

23-B1,23-B4,23-D3,23-E5
27-C1,27-C3,27-C4,27-D1
27-D2,27-D4,27-E1 — FPGA_DDR2_SDRAM_DQSN_NC[7:0]

23-B1,23-B4,23-E5,27-C1
27-D4,27-E1 — FPGA_DDR2_SDRAM_CK_P[1:0]

23-B1,23-B4,23-E5,27-C1
27-D4,27-E1 — FPGA_DDR2_SDRAM_CK_N[1:0]

23-B1,23-B4,23-C1,23-C4
23-D3,23-E3,23-E5,27-C1
27-C3,27-C4,27-D1,27-D2
27-D4,27-E1,27-E2 — FPGA_DDR2_SDRAM_DM[7:0]

24-C3,24-D5,27-A4,27-D1
27-D3 — FPGA_DDR2_SDRAM_SN[1:0]

24-C3,24-D5,27-A4,27-D1
27-D3 — FPGA_DDR2_SDRAM_ODT[1:0]

15-B5,15-C1,27-D1 — FPGA_DDR2_SDRAM_SDA

15-B5,15-C1,27-D1 — FPGA_DDR2_SCL

U42 — MT16HTF12864H SODIMM Connector (1 of 8)

P0V9D_SDRAM_VREF

	1	VREF	
	2	VSS_D0	
	3	VSS_D1	
FPGA_DDR2_SDRAM_DQ4	4	DQ4	
FPGA_DDR2_SDRAM_DQ0	5	DQ0	
FPGA_DDR2_SDRAM_DQ5	6	DQ5	
FPGA_DDR2_SDRAM_DQ1	7	DQ1	
	8	VSS_D2	
	9	VSS_D3	
FPGA_DDR2_SDRAM_DM0	10	DM0	
FPGA_DDR2_SDRAM_DQSN_NC0	11	DQS0#	
	12	VSS_D4	
FPGA_DDR2_SDRAM_DQS0	13	DQS0	
FPGA_DDR2_SDRAM_DQ6	14	DQ6	
	15	VSS_D5	
FPGA_DDR2_SDRAM_DQ7	16	DQ7	
FPGA_DDR2_SDRAM_DQ2	17	DQ2	
	18	VSS_D6	
FPGA_DDR2_SDRAM_DQ3	19	DQ3	
FPGA_DDR2_SDRAM_DQ12	20	DQ12	
	21	VSS_D7	
FPGA_DDR2_SDRAM_DQ13	22	DQ13	
FPGA_DDR2_SDRAM_DQ8	23	DQ8	
	24	VSS_D8	
FPGA_DDR2_SDRAM_DQ9	25	DQ9	

U42 — MT16HTF12864H SODIMM Connector (3 of 8)

FPGA_DDR2_SDRAM_DQS2	51	DQS2	
FPGA_DDR2_SDRAM_DM2	52	DM2	
	53	VSS_D0	
	54	VSS_D1	
FPGA_DDR2_SDRAM_DQ18	55	DQ18	
FPGA_DDR2_SDRAM_DQ22	56	DQ22	
FPGA_DDR2_SDRAM_DQ19	57	DQ19	
FPGA_DDR2_SDRAM_DQ23	58	DQ23	
	59	VSS_D2	
	60	VSS_D3	
FPGA_DDR2_SDRAM_DQ24	61	DQ24	
FPGA_DDR2_SDRAM_DQ28	62	DQ28	
FPGA_DDR2_SDRAM_DQ25	63	DQ25	
FPGA_DDR2_SDRAM_DQ29	64	DQ29	
	65	VSS_D4	
	66	VSS_D5	
FPGA_DDR2_SDRAM_DM3	67	DM3	
FPGA_DDR2_SDRAM_DQSN_NC3	68	DQS3#	
NC	69	NC_D0	
FPGA_DDR2_SDRAM_DQS3	70	DQS3	
	71	VSS_D6	
	72	VSS_D7	
FPGA_DDR2_SDRAM_DQ26	73	DQ26	
FPGA_DDR2_SDRAM_DQ30	74	DQ30	
FPGA_DDR2_SDRAM_DQ27	75	DQ27	

U42 — MT16HTF12864H SODIMM Connector (5 of 8)

P1V8D_SDRAM

FPGA_DDR2_SDRAM_A0	101	A1	
FPGA_DDR2_SDRAM_A1	102	A0	
	103	VDD_D0	
	104	VDD_D1	
FPGA_DDR2_SDRAM_A10	105	A10/AP	
FPGA_DDR2_SDRAM_BA1	106	BA1	
FPGA_DDR2_SDRAM_BA0	107	BA0	
FPGA_DDR2_SDRAM_RASN	108	RAS#	
FPGA_DDR2_SDRAM_WEN	109	WE#	
FPGA_DDR2_SDRAM_SN0	110	S0#	
	111	VDD_D2	
	112	VDD_D3	
FPGA_DDR2_SDRAM_CASN	113	CAS#	
FPGA_DDR2_SDRAM_ODT0	114	ODT0	
FPGA_DDR2_SDRAM_SN1	115	S1#	
FPGA_DDR2_SDRAM_A13	116	NC/A13	
	117	VDD_D4	
	118	VDD_D5	
FPGA_DDR2_SDRAM_ODT1	119	ODT1	
NC	120	NC_D0	
	121	VSS_D0	
	122	VSS_D1	
FPGA_DDR2_SDRAM_DQ32	123	DQ32	
FPGA_DDR2_SDRAM_DQ36	124	DQ36	
FPGA_DDR2_SDRAM_DQ33	125	DQ33	

U42 — MT16HTF12864H SODIMM Connector (7 of 8)

FPGA_DDR2_SDRAM_DQ42	151	DQ42	
FPGA_DDR2_SDRAM_DQ46	152	DQ46	
FPGA_DDR2_SDRAM_DQ43	153	DQ43	
FPGA_DDR2_SDRAM_DQ47	154	DQ47	
	155	VSS_D0	
	156	VSS_D1	
FPGA_DDR2_SDRAM_DQ48	157	DQ48	
FPGA_DDR2_SDRAM_DQ52	158	DQ52	
FPGA_DDR2_SDRAM_DQ49	159	DQ49	
FPGA_DDR2_SDRAM_DQ53	160	DQ53	
	161	VSS_D2	
	162	VSS_D3	
NC	163	NC_D0	
FPGA_DDR2_SDRAM_CK_P1	164	CK1	
	165	VSS_D4	
FPGA_DDR2_SDRAM_CK_N1	166	CK1#	
FPGA_DDR2_SDRAM_DQSN_NC6	167	DQS6#	
	168	VSS_D5	
FPGA_DDR2_SDRAM_DQS6	169	DQS6	
FPGA_DDR2_SDRAM_DM6	170	DM6	
	171	VSS_D6	
	172	VSS_D7	
FPGA_DDR2_SDRAM_DQ50	173	DQ50	
FPGA_DDR2_SDRAM_DQ54	174	DQ54	
FPGA_DDR2_SDRAM_DQ51	175	DQ51	

U42 — MT16HTF12864H SODIMM Connector (2 of 8)

FPGA_DDR2_SDRAM_DM1	26	DM1	
	27	VSS_D0	
	28	VSS_D1	
FPGA_DDR2_SDRAM_DQSN_NC1	29	DQS1#	
FPGA_DDR2_SDRAM_CK_P0	30	CK0	
FPGA_DDR2_SDRAM_DQS1	31	DQS1	
FPGA_DDR2_SDRAM_CK_N0	32	CK0#	
	33	VSS_D2	
	34	VSS_D3	
FPGA_DDR2_SDRAM_DQ10	35	DQ10	
FPGA_DDR2_SDRAM_DQ14	36	DQ14	
FPGA_DDR2_SDRAM_DQ11	37	DQ11	
FPGA_DDR2_SDRAM_DQ15	38	DQ15	
	39	VSS_D4	
	40	VSS_D5	
	41	VSS_D6	
	42	VSS_D7	
FPGA_DDR2_SDRAM_DQ16	43	DQ16	
FPGA_DDR2_SDRAM_DQ20	44	DQ20	
FPGA_DDR2_SDRAM_DQ17	45	DQ17	
FPGA_DDR2_SDRAM_DQ21	46	DQ21	
	47	VSS_D8	
	48	VSS_D9	
FPGA_DDR2_SDRAM_DQSN_NC2	49	DQS2#	
NC	50	NC_D0	

U42 — MT16HTF12864H SODIMM Connector (4 of 8)

P1V8D_SDRAM

FPGA_DDR2_SDRAM_DQ31	76	DQ31	
	77	VSS_D0	
	78	VSS_D1	
FPGA_DDR2_SDRAM_CKE0	79	CKE0	
FPGA_DDR2_SDRAM_CKE1	80	CKE1	
	81	VDD_D0	
	82	VDD_D1	
NC	83	NC_D0	
FPGA_DDR2_SDRAM_A15	84	NC_D1	
FPGA_DDR2_SDRAM_BA2	85	NC/BA2	
FPGA_DDR2_SDRAM_A14	86	NC_D2	
	87	VDD_D2	
	88	VDD_D3	
FPGA_DDR2_SDRAM_A12	89	A12	
FPGA_DDR2_SDRAM_A11	90	A11	
FPGA_DDR2_SDRAM_A9	91	A9	
FPGA_DDR2_SDRAM_A7	92	A7	
FPGA_DDR2_SDRAM_A8	93	A8	
FPGA_DDR2_SDRAM_A6	94	A6	
	95	VDD_D4	
	96	VDD_D5	
FPGA_DDR2_SDRAM_A5	97	A5	
FPGA_DDR2_SDRAM_A4	98	A4	
FPGA_DDR2_SDRAM_A3	99	A3	
FPGA_DDR2_SDRAM_A2	100	A2	

For self refresh

R135 10K
R136 10K

U42 — MT16HTF12864H SODIMM Connector (6 of 8)

FPGA_DDR2_SDRAM_DQ37	126	DQ37	
	127	VSS_D0	
	128	VSS_D1	
FPGA_DDR2_SDRAM_DQSN_NC4	129	DQS4#	
FPGA_DDR2_SDRAM_DM4	130	DM4	
FPGA_DDR2_SDRAM_DQS4	131	DQS4	
	132	VSS_D2	
	133	VSS_D3	
FPGA_DDR2_SDRAM_DQ38	134	DQ38	
FPGA_DDR2_SDRAM_DQ34	135	DQ34	
FPGA_DDR2_SDRAM_DQ39	136	DQ39	
FPGA_DDR2_SDRAM_DQ35	137	DQ35	
	138	VSS_D4	
	139	VSS_D5	
FPGA_DDR2_SDRAM_DQ44	140	DQ44	
FPGA_DDR2_SDRAM_DQ40	141	DQ40	
FPGA_DDR2_SDRAM_DQ45	142	DQ45	
FPGA_DDR2_SDRAM_DQ41	143	DQ41	
	144	VSS_D6	
	145	VSS_D7	
FPGA_DDR2_SDRAM_DQSN_NC5	146	DQS5#	
FPGA_DDR2_SDRAM_DM5	147	DM5	
FPGA_DDR2_SDRAM_DQS5	148	DQS5	
	149	VSS_D8	
	150	VSS_D9	

P3V3D_SDRAM

R218 1.5K
R219 4.75K

Pull-up required due to open drain interface

U42 — MT16HTF12864H SODIMM Connector (8 of 8)

P3V3D_SDRAM

FPGA_DDR2_SDRAM_DQ55	176	DQ55	
	177	VSS_D0	
	178	VSS_D1	
FPGA_DDR2_SDRAM_DQ56	179	DQ56	
FPGA_DDR2_SDRAM_DQ60	180	DQ60	
FPGA_DDR2_SDRAM_DQ57	181	DQ57	
FPGA_DDR2_SDRAM_DQ61	182	DQ61	
	183	VSS_D2	
	184	VSS_D3	
FPGA_DDR2_SDRAM_DM7	185	DM7	
FPGA_DDR2_SDRAM_DQSN_NC7	186	DQS7#	
	187	VSS_D4	
FPGA_DDR2_SDRAM_DQS7	188	DQS7	
FPGA_DDR2_SDRAM_DQS8	189	DQS8	
	190	VSS_D5	
FPGA_DDR2_SDRAM_DQ59	191	DQ59	
FPGA_DDR2_SDRAM_DQ62	192	DQ62	
	193	VSS_D6	
FPGA_DDR2_SDRAM_DQ63	194	DQ63	
FPGA_DDR2_SDRAM_SDA	195	SDA	
	196	VSS_D7	
FPGA_DDR2_SDRAM_SCL	197	SCL	
	198	SA0	
	199	VDDSPD	
	200	SA1	

B DDR2 Termination/Power Inputs

P3V3D — L115 56-OHM — P3V3D_SDRAM — C859 100U
P1V8D — L112 56-OHM — P1V8D_SDRAM — C858 100U
P0V9D_VREF — L113 56-OHM — P0V9D_SDRAM_VREF — C857 100U
P0V9D_VTT — L114 56-OHM — P0V9D_SDRAM_VTT — C854 100U

C DDR2 Termination Decoupling

P0V9D_SDRAM_VTT

Place DDR2 SDRAM termination Decoupling
near SODIMM. One 0.1uF capacitor per 2 VDD pins.

C855 100U

C330 0.1UF, C331 0.1UF, C316 0.1UF, C329 0.1UF, C327 0.1UF, C332 0.1UF

Place DDR2 SDRAM termination Decoupling near terminated signals.

C856 100U

C232 0.1UF, C231 0.1UF, C235 0.1UF, C233 0.1UF, C234 0.1UF, C315 0.1UF

D DDR2 Terminations

P0V9D_SDRAM_VTT

FPGA_DDR2_SDRAM_A15	R34	47
FPGA_DDR2_SDRAM_A14	R35	47
FPGA_DDR2_SDRAM_A13	R29	47
FPGA_DDR2_SDRAM_A12	R28	47
FPGA_DDR2_SDRAM_A11	R27	47
FPGA_DDR2_SDRAM_A10	R26	47
FPGA_DDR2_SDRAM_A9	R25	47
FPGA_DDR2_SDRAM_A8	R24	47
FPGA_DDR2_SDRAM_A7	R23	47
FPGA_DDR2_SDRAM_A6	R22	47
FPGA_DDR2_SDRAM_A5	R21	47
FPGA_DDR2_SDRAM_A4	R20	47
FPGA_DDR2_SDRAM_A3	R31	47
FPGA_DDR2_SDRAM_A2	R30	47
FPGA_DDR2_SDRAM_A1	R33	47
FPGA_DDR2_SDRAM_A0	R32	47

P0V9D_SDRAM_VTT

FPGA_DDR2_SDRAM_BA[2:0]

FPGA_DDR2_SDRAM_BA2	R36	47
FPGA_DDR2_SDRAM_BA1	R37	47
FPGA_DDR2_SDRAM_BA0	R38	47

FPGA_DDR2_SDRAM_SN[1:0]

FPGA_DDR2_SDRAM_SN1	R39	47
FPGA_DDR2_SDRAM_SN0	R40	47

FPGA_DDR2_SDRAM_ODT[1:0]

FPGA_DDR2_SDRAM_ODT1	R41	47
FPGA_DDR2_SDRAM_ODT0	R47	47

FPGA_DDR2_SDRAM_CKE[1:0]

FPGA_DDR2_SDRAM_CKE1	R46	47
FPGA_DDR2_SDRAM_CKE0	R45	47

FPGA_DDR2_SDRAM_CASN	R44	47
FPGA_DDR2_SDRAM_RASN	R43	47
FPGA_DDR2_SDRAM_WEN	R42	47

VLSI Computation LAB

Title:	DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 27 of 43 REV: 001

QDR-II SRAM - Address, Data, Control

Samsung K7R323684C-EC250

** INPUTS **

SRAM Write Data

23-B3,23-C3,23-C5,23-D5
24-D3,24-E5,28-B2,28-C2
28-E2,29-C4,29-E1 — FPGA_SRAM_WDATA[35:0]

SRAM Control

24-C3,24-E5,28-B2,28-E2
29-C4,29-E1 — FPGA_SRAM_WRN

24-C3,24-E5,28-B4,28-E2
29-C4,29-E1 — FPGA_SRAM_RDN

23-B3,23-C3,23-D5,23-E5
24-D3,24-E5,28-A2,28-B2
28-E2,29-C4,29-E1 — FPGA_SRAM_BWN[3:0]

24-C3,24-D3,24-E5,28-C7
28-E2,29-C3,29-E1 — FPGA_SRAM_ADDR[17:0]

SRAM Clocks

24-D3,24-E5,28-A2,28-D2
29-B3,29-E1 — FPGA_SRAM_K_CLK_P

24-D3,24-E5,28-A2,28-D2
29-B3,29-E1 — FPGA_SRAM_K_CLK_N

24-D3,24-D5,28-D2,29-B4
29-D1 — FPGA_SRAM_C_CLK_P

24-D3,24-D5,28-D2,29-B4
29-D1 — FPGA_SRAM_C_CLK_N

** OUTPUTS **

SRAM Read Data

FPGA_SRAM_RDATA[35:0] → 23-D4,23-E1,23-E4,28-B4
28-C4,28-E7

SRAM Read Clock

FPGA_SRAM_CQ_CLK_P → 23-D4,23-E1,28-A4,28-E7

FPGA_SRAM_CQ_CLK_N → 23-D4,23-E1,28-A4,28-E7

A QDR-II SRAM Read/Write Data

All data, address, clocks must have equal length lines

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FPGA_SRAM_WDATA0	P10	B2_D0	B3_Q0	P11	FPGA_SRAM_RDATA0
FPGA_SRAM_WDATA1	N11	B2_D1	B3_Q1	M10	FPGA_SRAM_RDATA1
FPGA_SRAM_WDATA2	M11	B2_D2	B3_Q2	L11	FPGA_SRAM_RDATA2
FPGA_SRAM_WDATA3	K10	B2_D3	B3_Q3	K11	FPGA_SRAM_RDATA3
FPGA_SRAM_WDATA4	J11	B2_D4	B3_Q4	J10	FPGA_SRAM_RDATA4
FPGA_SRAM_WDATA5	G11	B2_D5	B3_Q5	F11	FPGA_SRAM_RDATA5
FPGA_SRAM_WDATA6	E10	B2_D6	B3_Q6	E11	FPGA_SRAM_RDATA6
FPGA_SRAM_WDATA7	D11	B2_D7	B3_Q7	C10	FPGA_SRAM_RDATA7
FPGA_SRAM_WDATA8	C11	B2_D8	B3_Q8	B11	FPGA_SRAM_RDATA8
FPGA_SRAM_WDATA9	N10	B2_D9	B3_Q9	P9	FPGA_SRAM_RDATA9
FPGA_SRAM_WDATA10	M9	B2_D10	B3_Q10	N9	FPGA_SRAM_RDATA10
FPGA_SRAM_WDATA11	L9	B2_D11	B3_Q11	L10	FPGA_SRAM_RDATA11
FPGA_SRAM_WDATA12	J9	B2_D12	B3_Q12	K9	FPGA_SRAM_RDATA12
FPGA_SRAM_WDATA13	G10	B2_D13	B3_Q13	G9	FPGA_SRAM_RDATA13
FPGA_SRAM_WDATA14	F9	B2_D14	B3_Q14	F10	FPGA_SRAM_RDATA14
FPGA_SRAM_WDATA15	D10	B2_D15	B3_Q15	E9	FPGA_SRAM_RDATA15
FPGA_SRAM_WDATA16	C9	B2_D16	B3_Q16	D9	FPGA_SRAM_RDATA16
FPGA_SRAM_WDATA17	B9	B2_D17	B3_Q17	B10	FPGA_SRAM_RDATA17
FPGA_SRAM_WDATA18	B3	B2_D18	B3_Q18	B2	FPGA_SRAM_RDATA18
FPGA_SRAM_WDATA19	C3	B2_D19	B3_Q19	D3	FPGA_SRAM_RDATA19
FPGA_SRAM_WDATA20	D2	B2_D20	B3_Q20	E3	FPGA_SRAM_RDATA20
FPGA_SRAM_WDATA21	F3	B2_D21	B3_Q21	F2	FPGA_SRAM_RDATA21
FPGA_SRAM_WDATA22	G2	B2_D22	B3_Q22	G3	FPGA_SRAM_RDATA22
FPGA_SRAM_WDATA23	J3	B2_D23	B3_Q23	K3	FPGA_SRAM_RDATA23
FPGA_SRAM_WDATA24	L3	B2_D24	B3_Q24	L2	FPGA_SRAM_RDATA24
FPGA_SRAM_WDATA25	M3	B2_D25	B3_Q25	N3	FPGA_SRAM_RDATA25
FPGA_SRAM_WDATA26	N2	B2_D26	B3_Q26	P3	FPGA_SRAM_RDATA26
FPGA_SRAM_WDATA27	C1	B2_D27	B3_Q27	B1	FPGA_SRAM_RDATA27
FPGA_SRAM_WDATA28	D1	B2_D28	B3_Q28	C2	FPGA_SRAM_RDATA28
FPGA_SRAM_WDATA29	E2	B2_D29	B3_Q29	E1	FPGA_SRAM_RDATA29
FPGA_SRAM_WDATA30	G1	B2_D30	B3_Q30	F1	FPGA_SRAM_RDATA30
FPGA_SRAM_WDATA31	J1	B2_D31	B3_Q31	J2	FPGA_SRAM_RDATA31
FPGA_SRAM_WDATA32	K2	B2_D32	B3_Q32	K1	FPGA_SRAM_RDATA32
FPGA_SRAM_WDATA33	M1	B2_D33	B3_Q33	L1	FPGA_SRAM_RDATA33
FPGA_SRAM_WDATA34	N1	B2_D34	B3_Q34	M2	FPGA_SRAM_RDATA34
FPGA_SRAM_WDATA35	P2	B2_D35	B3_Q35	P1	FPGA_SRAM_RDATA35
FPGA_SRAM_WRN	A4	B2_W_N	B3_R_N	A8	FPGA_SRAM_RDN
FPGA_SRAM_BWN0	B7	B2_BW0_N			
FPGA_SRAM_BWN1	A7	B2_BW1_N			
FPGA_SRAM_BWN2	A5	B2_BW2_N			
FPGA_SRAM_BWN3	B5	B2_BW3_N			
FPGA_SRAM_K_CLK_P	B6	B2_K	B3_CQ	A11	FPGA_SRAM_CQ_CLK_P
FPGA_SRAM_K_CLK_N	A6	B2_K_N	B3_CQ_N	A1	FPGA_SRAM_CQ_CLK_N
FPGA_SRAM_C_CLK_P	P6	B2_C			
FPGA_SRAM_C_CLK_N	R6	B2_C_N			

P1V8D_SRAM

R590 NL

R591 NL

Adding 10Kohm Pull-Ups Disables C/CN clock at power up

B QDR-II SRAM Address

Use 0 Ohm Resistors in case
we use Cypress CY7C1415AV18,
Renesas R1Q3A3636ABG, or
NEC uPD44325364F5-E40-EQ2-A

All data, address, clocks must have equal length lines

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TMS_SRAM	R10	B0_TMS
TDI_SRAM	R11	B0_TDI
TCK_SRAM	R2	B0_TCK
TDO_SRAM	R1	B0_TDO
R675 249	H11	B0_ZQ
SRAM_DLL_OFFN	H1	B0_Doff_N
TP206 R589 NL	C6	B0_NC

B1_SA_D0	A9	FPGA_SRAM_ADDR0
B1_SA_D1	B4	FPGA_SRAM_ADDR1
B1_SA_D2	B8	FPGA_SRAM_ADDR2
B1_SA_D3	C5	FPGA_SRAM_ADDR3
B1_SA_D4	C7	FPGA_SRAM_ADDR4
B1_SA_D5	N5	FPGA_SRAM_ADDR5
B1_SA_D6	N6	FPGA_SRAM_ADDR6
B1_SA_D7	N7	FPGA_SRAM_ADDR7
B1_SA_D8	P4	FPGA_SRAM_ADDR8
B1_SA_D9	P5	FPGA_SRAM_ADDR9
B1_SA_D10	P7	FPGA_SRAM_ADDR10
B1_SA_D11	P8	FPGA_SRAM_ADDR11
B1_SA_D12	R3	FPGA_SRAM_ADDR12
B1_SA_D13	R4	FPGA_SRAM_ADDR13
B1_SA_D14	R5	FPGA_SRAM_ADDR14
B1_SA_D15	R7	FPGA_SRAM_ADDR15
B1_SA_D16	R8	FPGA_SRAM_ADDR16
B1_SA_D17	R9	FPGA_SRAM_ADDR17
B1_NC/SA_D18	A3	TP250
B1_NC/SA_D19	A10	TP251
B1_NC/SA_D20	A2	TP276

QDR II SRAM JTAG Interface

P1V8D_SRAM

C559 0.1U

R713 1.91K

R712 1.91K

VERT

J39 87832-1420

NC

NC

TMS_SRAM

TCK_SRAM

TDO_SRAM

TDI_SRAM

R711 1.91K

Jumper Settings:

DLL Enabled (VCC default)

DLL Disabled (GND)

P1V8D_SRAM

R48 499

SRAM_DLL_OFFN

P5F

VLSI Computation LAB

Title:	QDR-II SRAM - ADDRESS, DATA, CONTROL			
File:	MEAS_MAIN_BOARD			
Created by:	JEREMY W. WEBB		Date:	6-20-2008_16:40
Modified by:			Date:	
PCB NO:	342	Size: D	Sheet 28 of 43	REV: 001

QDR-II SRAM - Power and Terminations

Samsung K7R323684C-EC250

** INPUTS **

SRAM Write Data

23-B3,23-C3,23-C5,23-D5
24-D3,24-E5,28-B2,28-C2
28-E1,28-E2,29-C4,29-E1
FPGA_SRAM_WDATA[35:0]

SRAM Control

24-C3,24-E5,28-B2,28-E1
28-E2,29-C4,29-E1
FPGA_SRAM_WRN

24-C3,24-E5,28-B4,28-E1
28-E2,29-C4,29-E1
FPGA_SRAM_RDN

23-B3,23-C3,23-D5,23-E5
24-D3,24-E5,28-A2,28-B2
28-E1,28-E2,29-C4,29-E1
FPGA_SRAM_BWN[3:0]

24-C3,24-D3,24-E5,28-C7
28-E1,28-E2,29-C3,29-E1
FPGA_SRAM_ADDR[17:0]

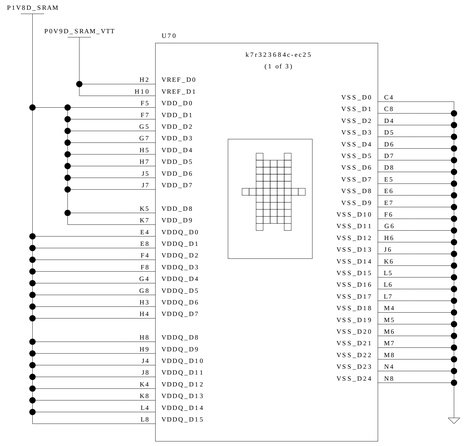
SRAM Clocks

24-D3,24-E5,28-A2,28-D1
28-D2,29-B3,29-E1
FPGA_SRAM_K_CLK_P

24-D3,24-E5,28-A2,28-D1
28-D2,29-B3,29-E1
FPGA_SRAM_K_CLK_N

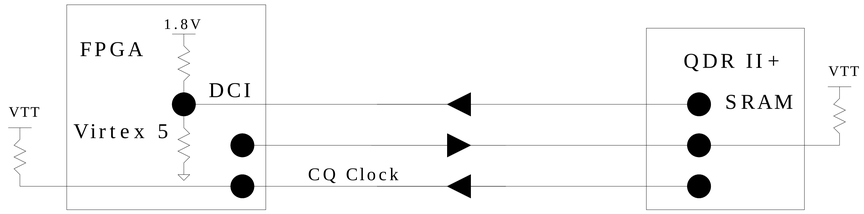
24-D3,24-D5,28-D1,28-D2
28-E1,28-E2,29-B4,29-D1
FPGA_SRAM_C_CLK_P

24-D3,24-D5,28-D1,28-D2
28-E1,28-E2,29-B4,29-D1
FPGA_SRAM_C_CLK_N



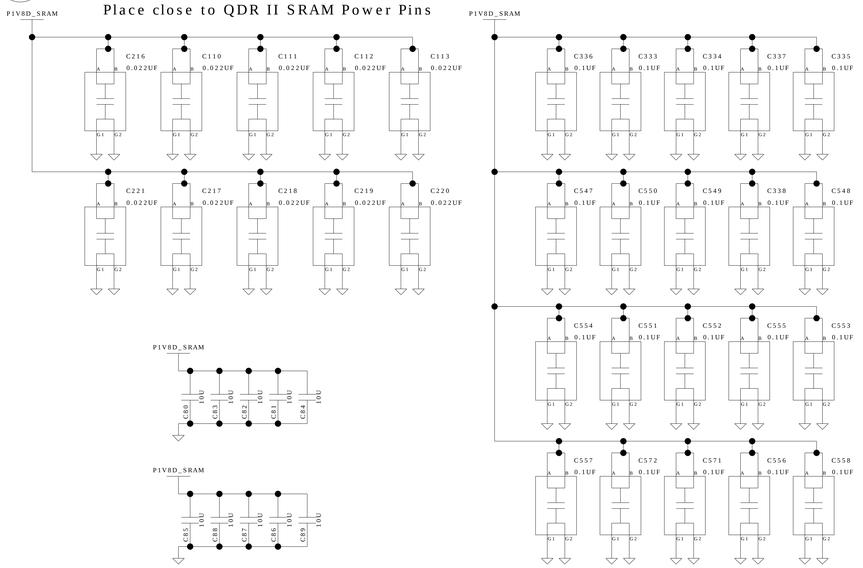
SRAM Termination Placement:

Place parallel terminations just beyond the SRAM and FPGA.

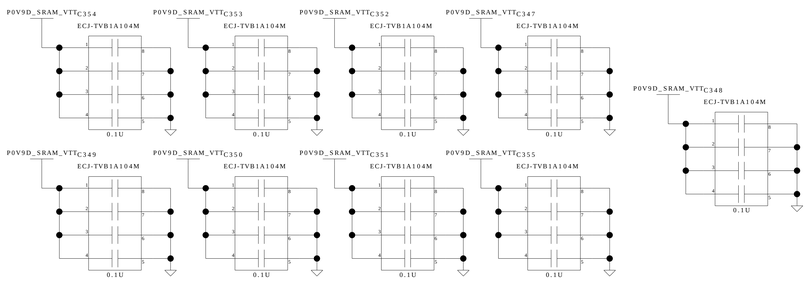


A QDR-II SRAM Decoupling

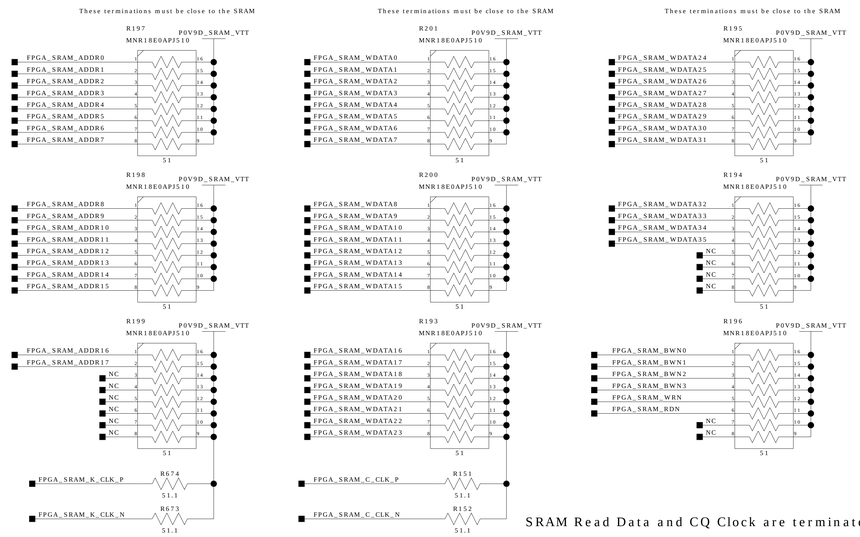
Place close to QDR II SRAM Power Pins



B QDR-II SRAM Termination Decoupling

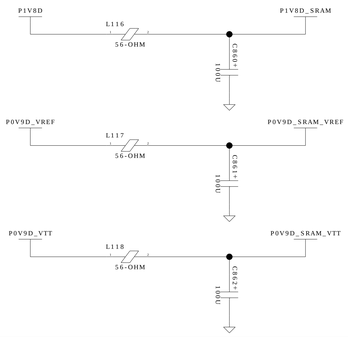


C QDR-II SRAM Write Data, Address Terminations



SRAM Read Data and CQ Clock are terminated at Virtex 5 FPGA using DCI HSTL_I_DCI_18.

D QDR-II Power Inputs



VLSI Computation LAB

Title:	QDR II SRAM - POWER AND TERMINATIONS		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 29 of 43	REV: 001

Xilinx Virtex-5 SX50T FPGA Peripherals

** INPUTS **

MicroSD Interface
- 22-C3,22-E5,30-E1 — FPGA_V5_SD_TXD
- 22-C3,22-E5,30-E1 — FPGA_V5_SD_CLK
- 22-C3,22-E5,30-E1 — FPGA_V5_SD_CARD_DETECT
- 22-C3,22-E5,30-B4,30-E1 — FPGA_V5_SD_BUSY_LED

USB to RS-232
- 22-D3,22-E5,30-E1 — FPGA_V5_RS232_TX
- 22-D3,22-E5,30-E1 — FPGA_V5_RS232_CTS

FT245BL USB Interface
- 22-D5,22-E3,30-C4,30-E1 — FPGA_V5_FTDI_RDN
- 22-D5,22-E3,30-C4,30-E1 — FPGA_V5_FTDI_WRN
- 22-D5,22-E3,30-C4,30-E1 — FPGA_V5_FTDI_SI_WU

Logic Analyzer
- 22-D2,22-D5,30-B5,30-E1 — FPGA_V5_LA_CLK
- 22-C2,22-D2,22-D5,30-B5 30-E1 — FPGA_V5_LA_DATA[7:0]

** OUTPUTS **

USB to RS-232 Interface
- FPGA_V5_RS232_RTS — 22-D1,22-D3,30-E5
- FPGA_V5_RS232_RX — 22-D1,22-D3,30-E5

Debug LEDs
- FPGA_V5_LEDS[3:0] — 22-D1,22-D3,30-C2,30-E5

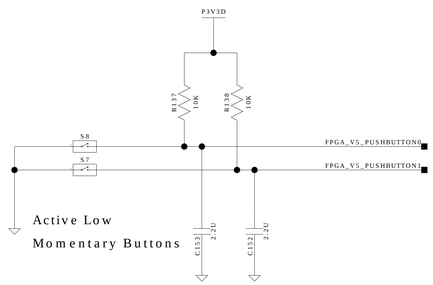
Debug Push Buttons
- FPGA_V5_PUSHBUTTON[1:0] — 22-C2,22-D1,30-C2,30-E5

MicroSD Interface
- FPGA_V5_SD_RXD — 22-C3,22-D1,30-E5

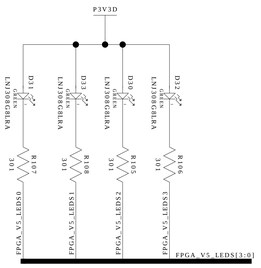
100MHz FPGA Clock
- FPGA_V5_CLK100MHZ_P — 22-C3,22-D1,30-B3,30-E5
- FPGA_V5_CLK100MHZ_N — 22-C3,22-D1,30-B3,30-D5

FT245BL USB Interface
- FPGA_V5_FTDI_DATA[7:0] — 22-C1,22-D3,22-E3,30-C5
- FPGA_V5_FTDI_TXEN — 22-C1,22-E3,30-C4,30-D5
- FPGA_V5_FTDI_RXFN — 22-C1,22-E3,30-C4,30-D5
- FPGA_V5_FTDI_PWRENN — 22-C1,22-E3,30-C4,30-D5
- FPGA_V5_FTDI_RSTOUTN — 22-C1,22-E3,30-D5

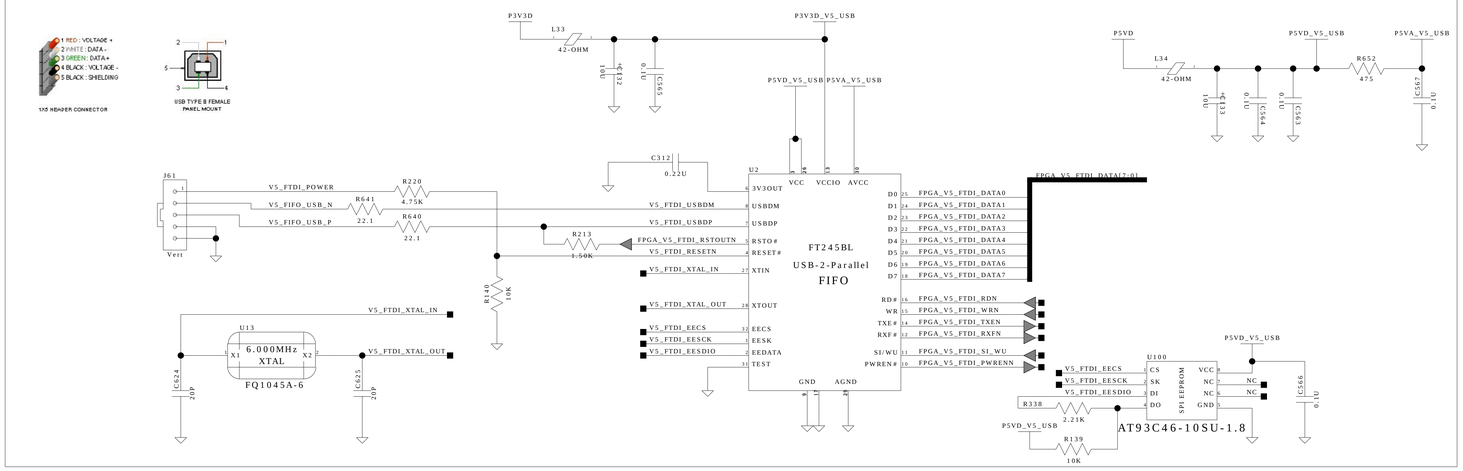
A PUSH-BUTTONs



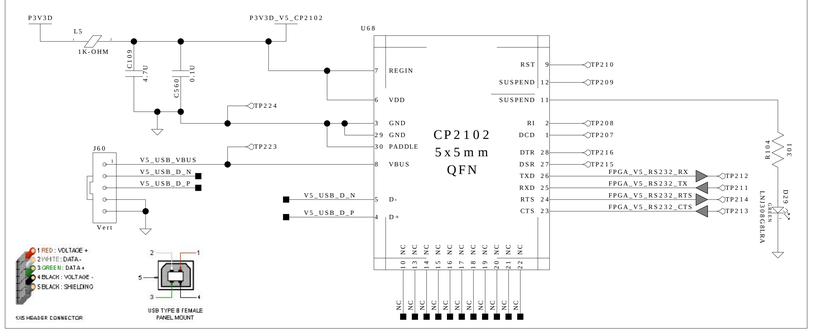
B DEBUG LEDs



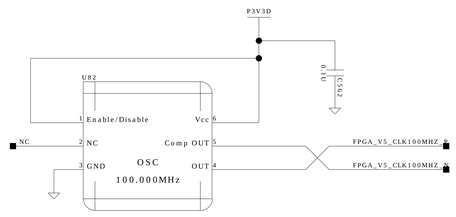
C USB Type-B Peripheral (Back-Up)



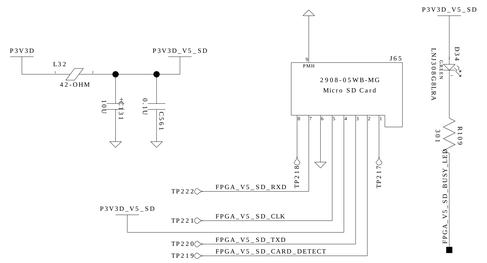
D USB-to-RS-232 Debug Interface



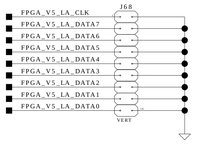
E 100MHz Digital Clock



F micro SD Card (2GB)



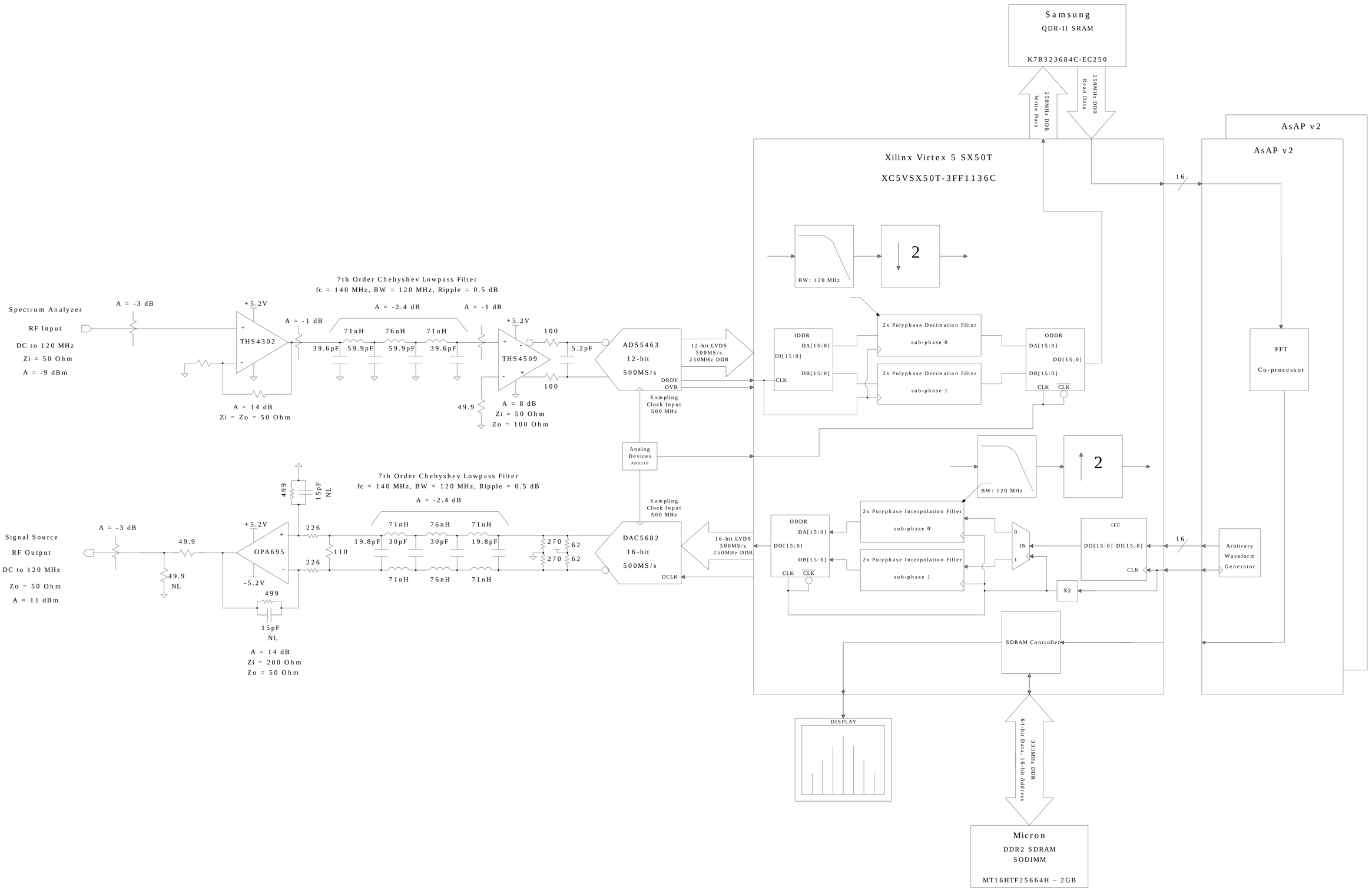
G LA HEADER



VLSI Computation LAB

Title:	XILINX VIRTEX-5 SX50T FPGA PERIPHERALS		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 30 of 43	REV: 001

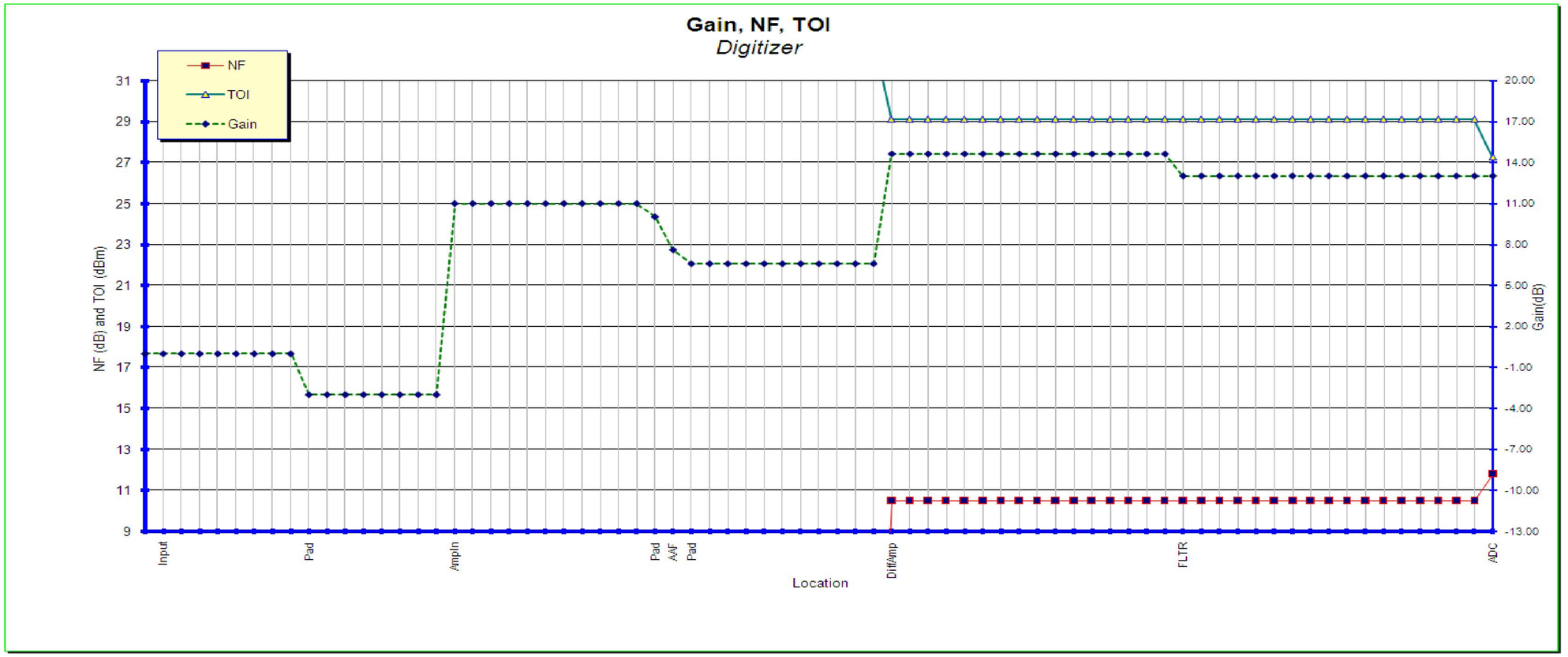
Spectrum Analyzer IF and Signal Source Block Diagrams

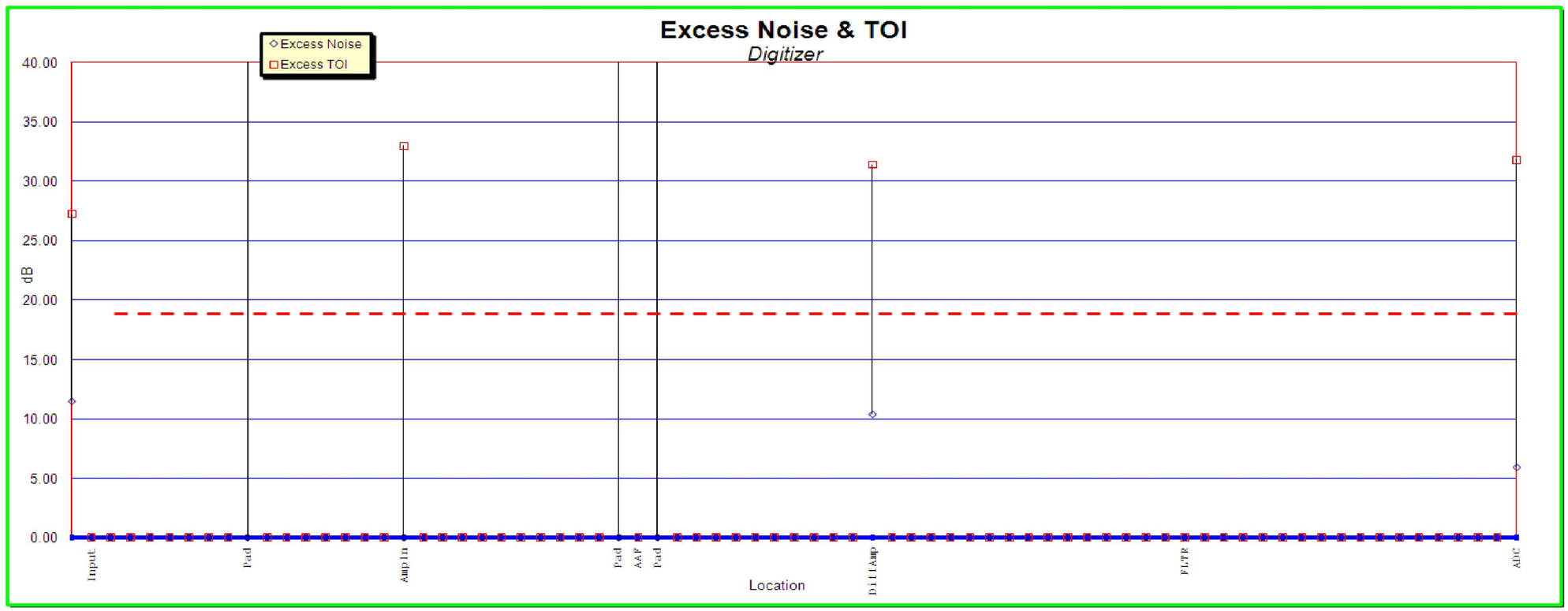


VLSI Computation LAB

Title:	SPECTRUM ANALYZER IF AND SIGNAL SOURCE BLOCK DIAGRAMS		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 31 of 43	REV: 001

Spectrum Analyzer IF Estimated Performance



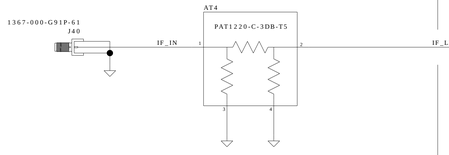


VLSI Computation LAB

Title:	SPECTRUM ANALYZER IF ESTIMATED PERFORMANCE		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 32 of 43 REV: 001

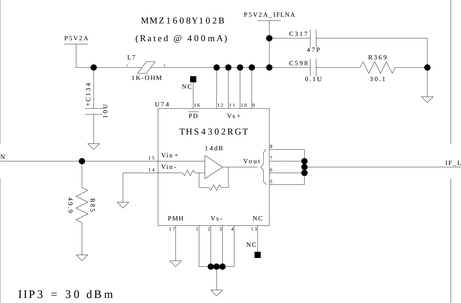
SPECTRUM ANALYZER IF

A 3dB Pad



Zi=Zo=50 Ohms
A = -3 dB +/- 0.3 dB
NF = 3 dB +/- 0.3 dB

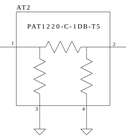
B LNA (+14 dBm)



IIP3 = 30 dBm
NF = 16 dB
A = +14 dB
+5V Analog: I = 190mA Max

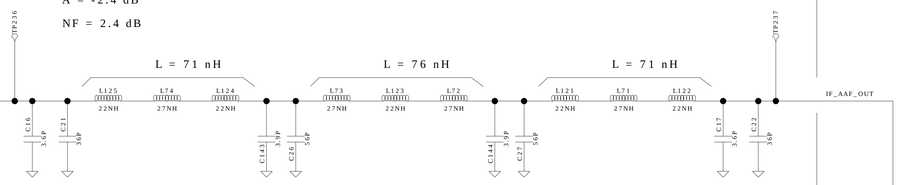
C 1dB PAD

Zi=Zo=50 Ohms
A = -1 dB +/- 0.3 dB
NF = 1 dB +/- 0.3 dB



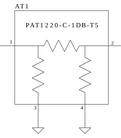
D Anti-Alias Filter

7th order Chebyshev Lowpass Filter
fc = 140 MHz, BW = 120 MHz, and Ripple = 0.5 dB
A = -2.4 dB
NF = 2.4 dB



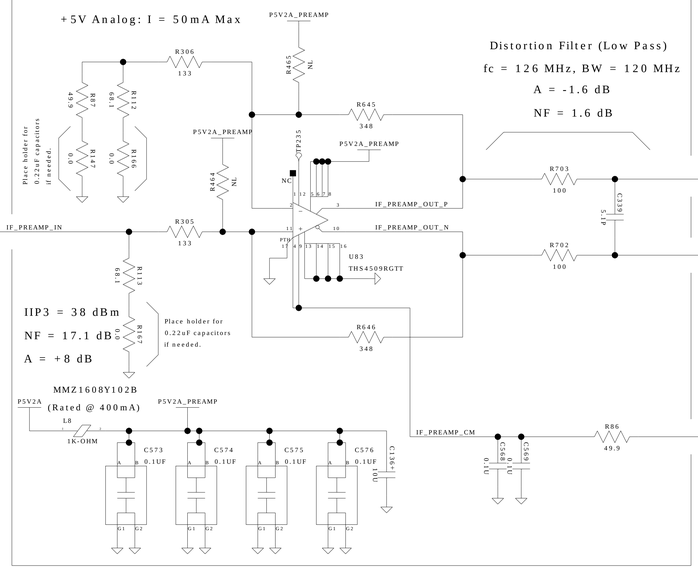
E 1dB PAD

Zi=Zo=50 Ohms
A = -1 dB +/- 0.3 dB
NF = 1 dB +/- 0.3 dB

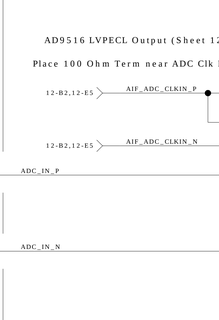


F Pre-Amplifier (+8 dBm)

+5V Analog: I = 50mA Max

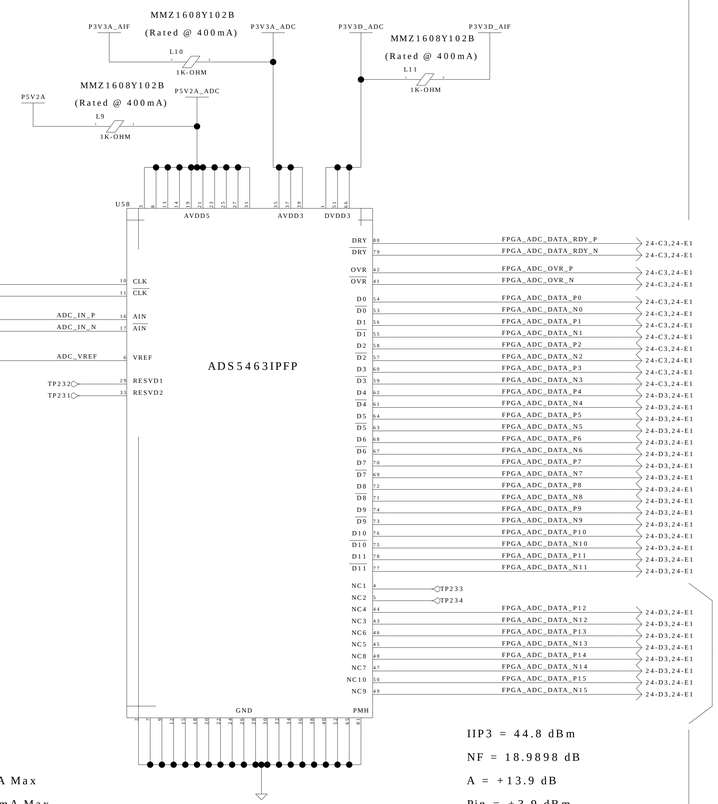


Distortion Filter (Low Pass)
fc = 126 MHz, BW = 120 MHz
A = -1.6 dB
NF = 1.6 dB



AD9516 LVPECL Output (Sheet 12)
Place 100 Ohm Term near ADC Clk Pins

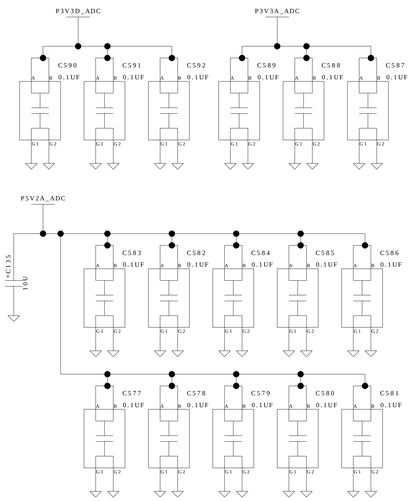
G High-Speed ADC (12-bit, 500MS/s)



+5V Analog: I = 330mA Max
+3.3V Analog: I = 138mA Max
+3.3V Digital: I = 88mA Max

IIP3 = 44.8 dBm
NF = 18.9898 dB
A = +13.9 dB
Pin = +3.9 dBm
FS = 2Vpp

H High-Speed ADC Decoupling



ADC PC Layout Notes:

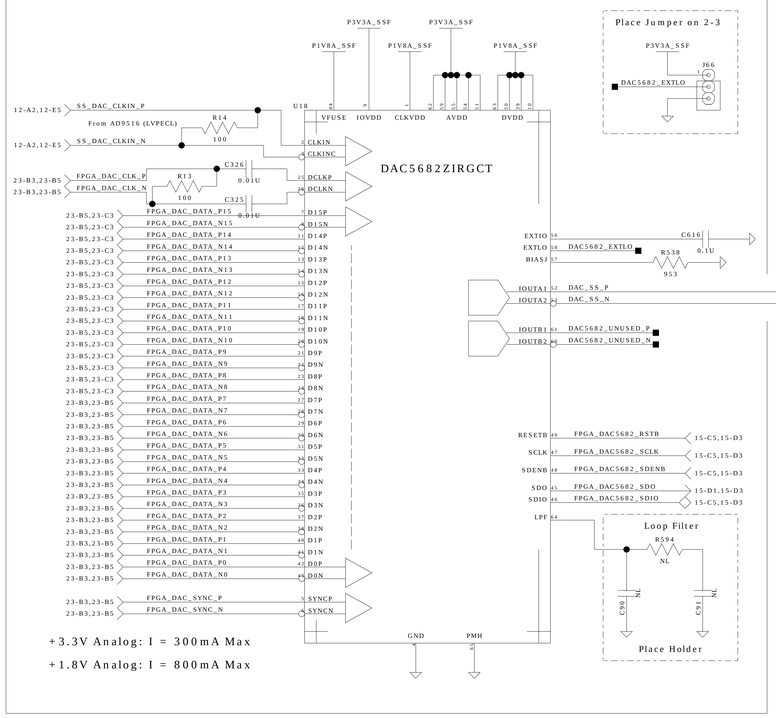
1. Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
2. It is recommended to place a small number of 25-mil-diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
3. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
4. Do not use the typical web or spoke via-connection pattern when connecting the thermal vias to the ground plane. Flood the via, rather than using a spoke pattern.

VLSI Computation LAB

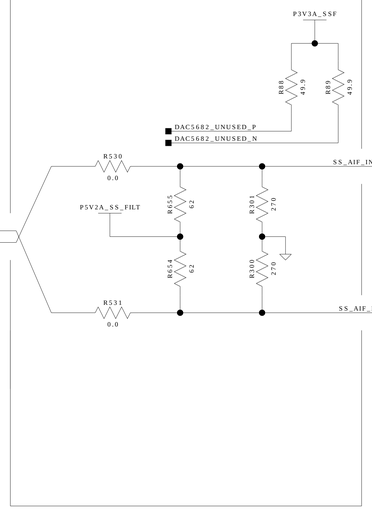
Title:	SPECTRUM ANALYZER IF		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 33 of 43	REV: 001

SIGNAL SOURCE

A High-Speed DAC (16-bits, 1GS/s)



B Output Stage



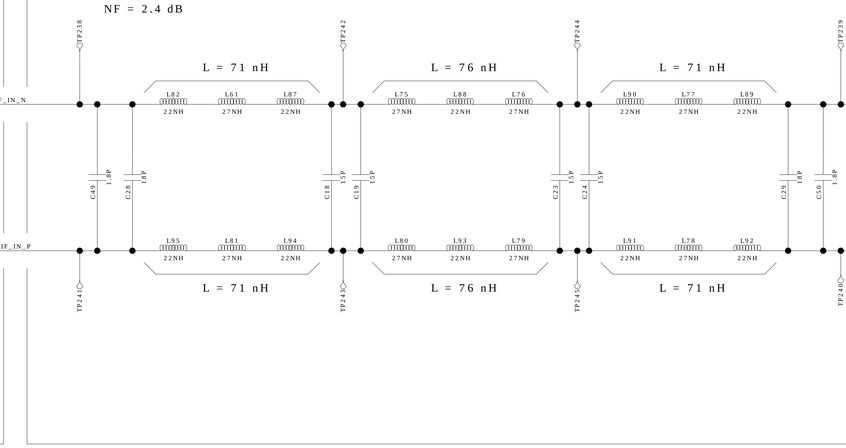
C Anti-Image Filter

7th order Chebyshev Lowpass Filter

fc = 140 MHz, BW = 120 MHz, and Ripple = 0.5 dB

A = -2.4 dB

NF = 2.4 dB



D Amplifier

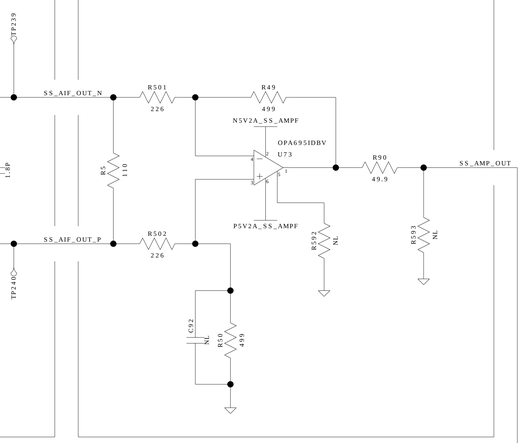
IIP3 = 20 dBm

NF = 14 dB

A = +14 dB

+5V Analog: I = 100mA Max

-5V Analog: I = 100mA Max

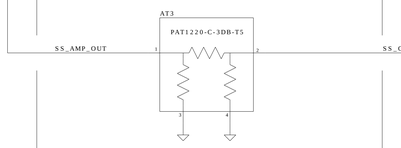


E 3dB PAD

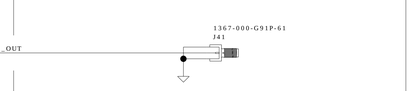
Zi=Zo=50 Ohms

A = -3 dB +/- 0.3 dB

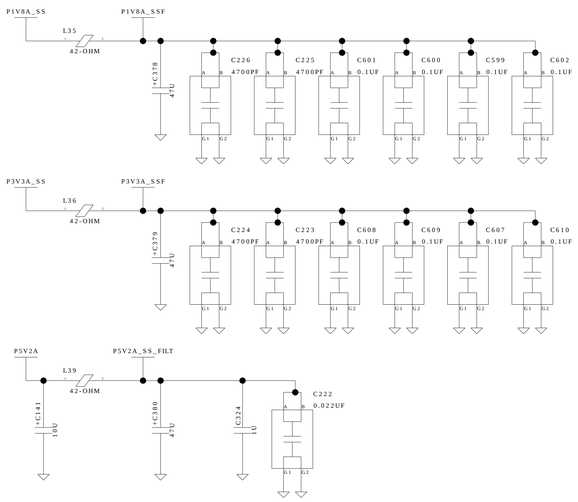
NF = 3 dB +/- 0.3 dB



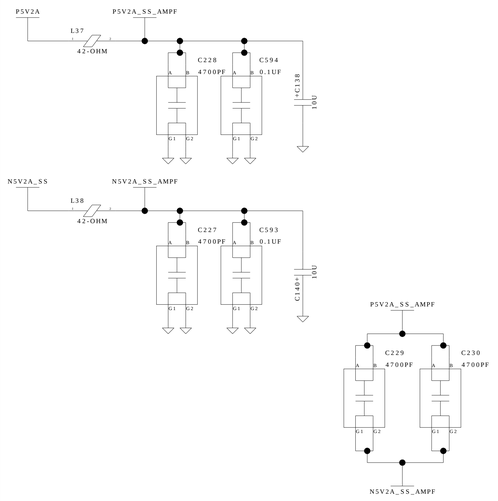
F Signal Source Output



G DAC5682 Decoupling



H OPA695 Decoupling



VLSI Computation LAB

Title:	SIGNAL SOURCE		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 34 of 43	REV: 001

Trigger Input/Output and Auxiliary Input

** INPUTS **

Trigger Output

22-D3,22-D5,35-D3,35-E1 — FPGA_TRIG_OUT_P
22-D3,22-D5,35-D3,35-E1 — FPGA_TRIG_OUT_N

** OUTPUTS **

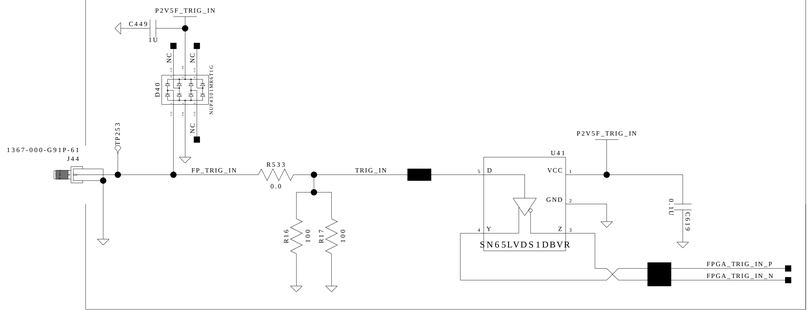
Auxiliary Input

FPGA_AUX_IN_P — 22-D1,22-D3,35-B3,35-E5
FPGA_AUX_IN_N — 22-D1,22-D3,35-B3,35-E5

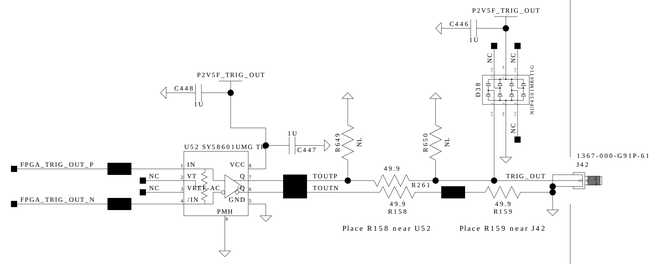
Trigger Input

FPGA_TRIG_IN_P — 22-C1,22-D3,35-D3,35-E5
FPGA_TRIG_IN_N — 22-C1,22-D3,35-D3,35-E5

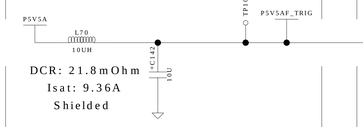
A Trigger Input Buffer



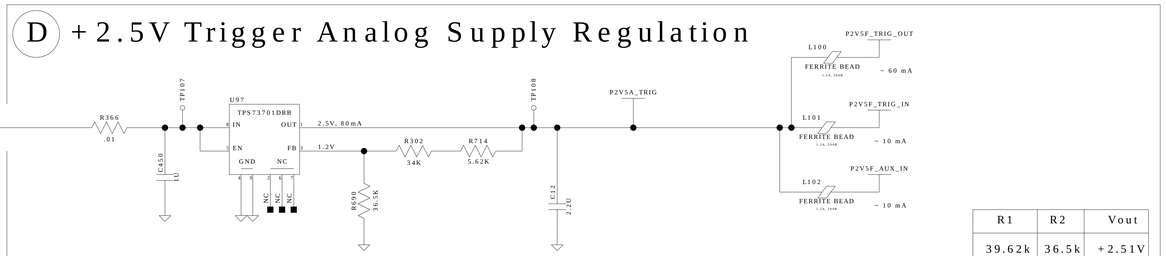
B Trigger Output Buffer



C +5.5V Filter

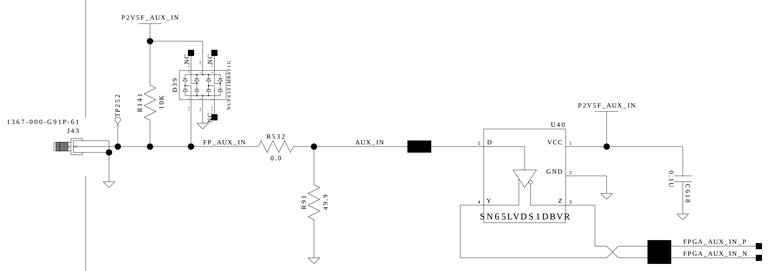


D +2.5V Trigger Analog Supply Regulation



R1	R2	Vout
39.62k	36.5k	+2.51V

E Auxillary Input



VLSI Computation LAB

Title:	TRIGGER INPUT/OUTPUT AND AUXILIARY INPUT		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 35 of 43	REV: 001

AsAPv2 #1 Data In/Out, Config, Analog, Test

** INPUTS **

AsAP 1 Data Output

23-C5,23-D3,36-C4,36-E1 — FPGA_ASAP1_REQ_OUT

AsAP 1 Data Input

23-C5,23-D3,23-E3,36-D3 36-E1,37-C2,37-C4,37-D1 — FPGA_ASAP1_DATA_IN[15:0]

23-C5,23-D3,36-D3,**37-D2** — FPGA_ASAP1_CLK_IN

23-B5,23-C5,23-D3,36-C4,36-D4,36-E1,37-B2,37-D1,37-D2 — FPGA_ASAP1_VLD_IN

AsAP 1 Config Input

15-B5,15-D3,36-D1,36-E1 — FPGA_ASAP1_RESET_COLD
15-B5,15-D3,36-C1,36-E1 — FPGA_ASAP1_CFG_CLK
15-B5,15-D3,36-C1,36-E1 — FPGA_ASAP1_CFG_VALID
15-B5,15-D3,36-C1,36-E1 — FPGA_ASAP1_SPI_CLK
15-B5,15-D3,36-D2,36-E1 — FPGA_ASAP1_SPI_CSN
15-B5,15-D3,36-C2,36-E1 — FPGA_ASAP1_SPI_LOAD
15-B5,15-D3,36-C2,36-E1 — FPGA_ASAP1_MOSI
15-B5,15-D3,36-B5,36-E1 — FPGA_ASAP1_RST_CNTCLK

** OUTPUTS **

AsAP 1 Data Output

FPGA_ASAP1_DATA_OUT[15:0] — 23-D3,23-E1,36-D4,36-E5
FPGA_ASAP1_CLK_OUT — 23-D3,23-E1,36-D4,36-E5
FPGA_ASAP1_VLD_OUT — 23-D3,23-E1,36-C4,36-E5

AsAP 1 Data Input

FPGA_ASAP1_REQ_IN — 23-D3,23-E1,36-C3,36-E5

AsAP 1 Config Output

FPGA_ASAP1_MISO — 15-C1,15-D3,36-C2,36-E5

A AsAP Config Level Translate

U101 SN74LVC1G07DBV: C611 0.1U; P2V5D; R149 294 1% 1/16W; FPGA_ASAP1_RESET_COLD → ASAP1_RESET_COLD
U105 SN74LVC1G07DBV: C362 0.1U; P2V5D; R304 294 1% 1/16W; FPGA_ASAP1_SPI_CSN → ASAP1_SPI_CSN
U102 SN74LVC1G07DBV: C359 0.1U; P2V5D; R150 294 1% 1/16W; FPGA_ASAP1_CFG_CLK → ASAP1_CFG_CLK
U106 SN74LVC1G07DBV: C358 0.1U; P2V5D; R294 294 1% 1/16W; FPGA_ASAP1_SPI_LOAD → ASAP1_SPI_LOAD
U103 SN74LVC1G07DBV: C357 0.1U; P2V5D; R131 294 1% 1/16W; FPGA_ASAP1_CFG_VALID → ASAP1_CFG_VALID
U107 SN74LVC1G07DBV: C356 0.1U; P3V3D; R84 402 1% 1/16W; ASAP1_SPI_MISO → FPGA_ASAP1_MISO
U104 SN74LVC1G07DBV: C194 0.1U; P2V5D; R408 294 1% 1/16W; FPGA_ASAP1_SPI_CLK → ASAP1_SPI_CLK
U108 SN74LVC1G07DBV: C195 0.1U; P2V5D; R168 294 1% 1/16W; FPGA_ASAP1_MOSI → ASAP1_SPI_MOSI

B AsAP Main Data Input and Output

U43 — vcl-asapv2-sbga304 (2 of 9)

FPGA_ASAP1_CLK_IN	N2	B0_IN_CLK	B1_OUT_CLK	K20	FPGA_ASAP1_CLK_OUT
FPGA_ASAP1_DATA_IN0	C2	B0_IN_DATA0	B1_OUT_DATA0	E20	FPGA_ASAP1_DATA_OUT0
FPGA_ASAP1_DATA_IN1	D3	B0_IN_DATA1	B1_OUT_DATA1	E21	FPGA_ASAP1_DATA_OUT1
FPGA_ASAP1_DATA_IN2	D2	B0_IN_DATA2	B1_OUT_DATA2	E22	FPGA_ASAP1_DATA_OUT2
FPGA_ASAP1_DATA_IN3	E4	B0_IN_DATA3	B1_OUT_DATA3	F20	FPGA_ASAP1_DATA_OUT3
FPGA_ASAP1_DATA_IN4	G3	B0_IN_DATA4	B1_OUT_DATA4	H20	FPGA_ASAP1_DATA_OUT4
FPGA_ASAP1_DATA_IN5	J2	B0_IN_DATA5	B1_OUT_DATA5	H21	FPGA_ASAP1_DATA_OUT5
FPGA_ASAP1_DATA_IN6	K1	B0_IN_DATA6	B1_OUT_DATA6	F23	FPGA_ASAP1_DATA_OUT6
FPGA_ASAP1_DATA_IN7	K2	B0_IN_DATA7	B1_OUT_DATA7	G23	FPGA_ASAP1_DATA_OUT7
FPGA_ASAP1_DATA_IN8	N3	B0_IN_DATA8	B1_OUT_DATA8	J22	FPGA_ASAP1_DATA_OUT8
FPGA_ASAP1_DATA_IN9	R1	B0_IN_DATA9	B1_OUT_DATA9	P21	FPGA_ASAP1_DATA_OUT9
FPGA_ASAP1_DATA_IN10	T1	B0_IN_DATA10	B1_OUT_DATA10	P20	FPGA_ASAP1_DATA_OUT10
FPGA_ASAP1_DATA_IN11	U1	B0_IN_DATA11	B1_OUT_DATA11	P23	FPGA_ASAP1_DATA_OUT11
FPGA_ASAP1_DATA_IN12	V1	B0_IN_DATA12	B1_OUT_DATA12	T23	FPGA_ASAP1_DATA_OUT12
FPGA_ASAP1_DATA_IN13	AA1	B0_IN_DATA13	B1_OUT_DATA13	W22	FPGA_ASAP1_DATA_OUT13
FPGA_ASAP1_DATA_IN14	Y3	B0_IN_DATA14	B1_OUT_DATA14	Y23	FPGA_ASAP1_DATA_OUT14
FPGA_ASAP1_DATA_IN15	AC3	B0_IN_DATA15	B1_OUT_DATA15	Y20	FPGA_ASAP1_DATA_OUT15
FPGA_ASAP1_REQ_IN	P4	B0_IN_REQUEST	B1_OUT_REQUEST	L22	FPGA_ASAP1_REQ_OUT
FPGA_ASAP1_VLD_IN	N1	B0_IN_VALID	B1_OUT_VALID	L21	FPGA_ASAP1_VLD_OUT
ASAP1_EXT_CLK_IN	AC10	B0_EXTERNAL_CLK			

142-0701-231 J25 — R92 49.9 — ASAP1_EXT_CLK_IN

C AsAP Configuration and Test Port

Place 30.1 Ohm Series Resistor on AsAP SPI_MISO near AsAp IC.

Place 30.1 Ohm Series Resistors on all other SPI, CFG, and Reset Cold signals near FPGA Outputs

U43 — vcl-asapv2-sbga304 (3 of 9)

ASAP1_RESET_COLD	Y11	B2_RESET_COLD	B3_TEST_OUT0	AB14	ASAP1_TEST_OUT0	R416 30.1 ASAP1_TEST0
ASAP1_CFG_CLK	AC11	B2_CFG_CLK	B3_TEST_OUT1	AA14	ASAP1_TEST_OUT1	R418 30.1 ASAP1_TEST1
ASAP1_CFG_VALID	AB11	B2_CFG_VALID	B3_TEST_OUT2	Y14	ASAP1_TEST_OUT2	R417 30.1 ASAP1_TEST2
ASAP1_SPI_CLK	AB7	B2_SPI_CLK	B3_TEST_OUT3	AC15	ASAP1_TEST_OUT3	R419 30.1 ASAP1_TEST3
ASAP1_SPI_CSN	AB5	B2_SPI_SEL	B3_TEST_OUT4	Y17	ASAP1_TEST_OUT4	R420 30.1 ASAP1_TEST4
ASAP1_SPI_LOAD	AB6	B2_SPI_LOAD	B3_TEST_OUT5	AB18	ASAP1_TEST_OUT5	R422 30.1 ASAP1_TEST5
ASAP1_SPI_MISO	AA7	B2_SPI_MISO	B3_TEST_OUT6	AA18	ASAP1_TEST_OUT6	R421 30.1 ASAP1_TEST6
ASAP1_SPI_MOSI	AC5	B2_SPI_MOSI	B3_TEST_OUT7	AC19	ASAP1_TEST_OUT7	R424 30.1 ASAP1_TEST7
			B3_TEST_OUT8	AC21	ASAP1_TEST_OUT8	R423 30.1 ASAP1_TEST8

TP256 TP257 TP258 TP259 TP260 TP261 TP262 TP263

J62 PBC05DAAN: ASAP1_TEST0–4 ↔ ASAP1_TEST8–5; VERT; NC

D AsAp Analog and Miscellaneous I/O

U43 — vcl-asapv2-sbga304 (9 of 9)

TP229	ASAP1_ANLG1	A8	B14_ANAG1	B15_TEMP_DIODE	B11 — TP255
TP228	ASAP1_ANLG2	A9	B14_ANAG2	B15_ANAREXT	C11 — R367 124K — TP254
TP227	ASAP1_ANLG3	A10	B14_ANAG3	B15_SPECIALGND	D11
TP230	ASAP1_ANLG4	A11	B14_ANAG4	B15_NC_00	J3
TP65				B15_NC_01	J4
TP64				B15_RESET_COUNTCLK	AA11 — ASAP1_RST_CNTCLK; TP264; R534 0.0; R535 0.0

ASAP1_RST_CNTCLK — R425 30.1 — FPGA_ASAP1_RST_CNTCLK

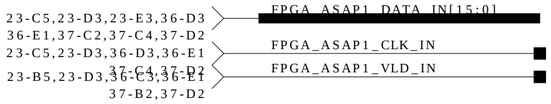
VLSI Computation LAB

Title:	ASAPV2 #1 DATA IN/OUT, CONFIG, ANALOG, TEST		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 36 of 43	REV: 001

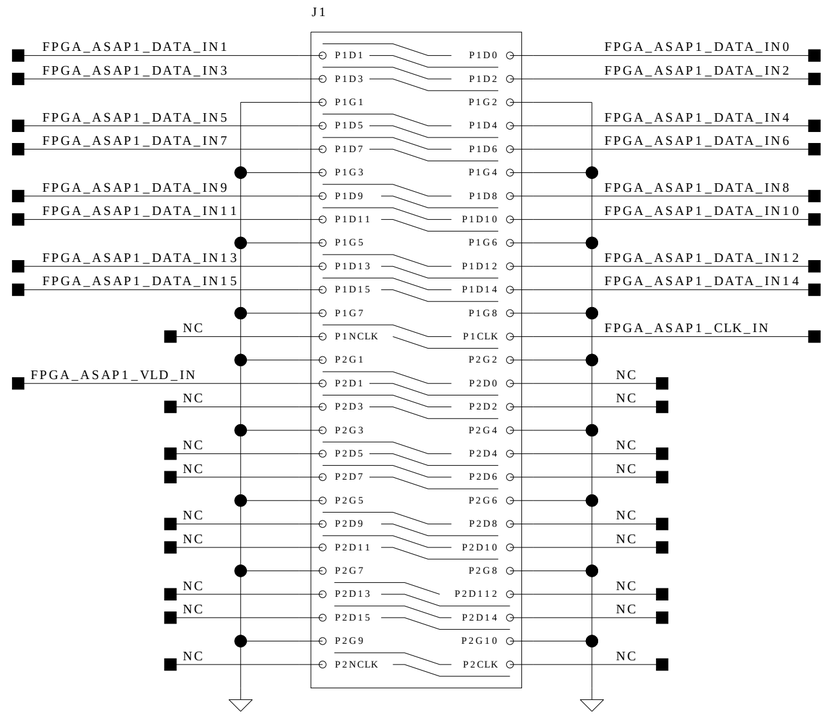
AGILENT 16902A Logic Analyzer E5390A SOFT-TOUCH CONNECTOR

** INPUTS **

AsAP 1 Data Input to Logic Analyzer



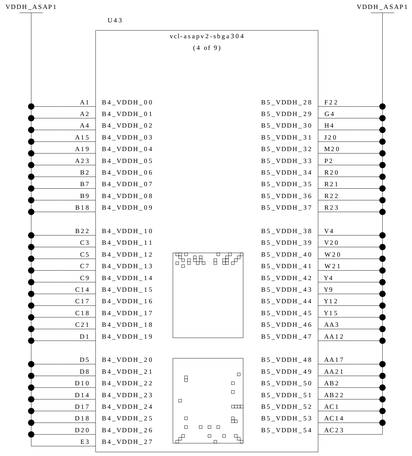
A SOFT-TOUCH SINGLE-ENDED PROBE (E5390A)

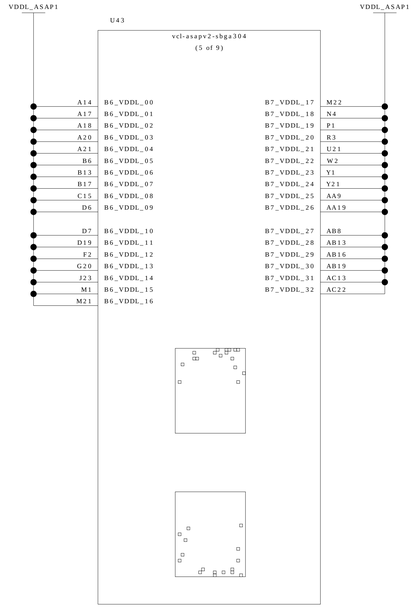


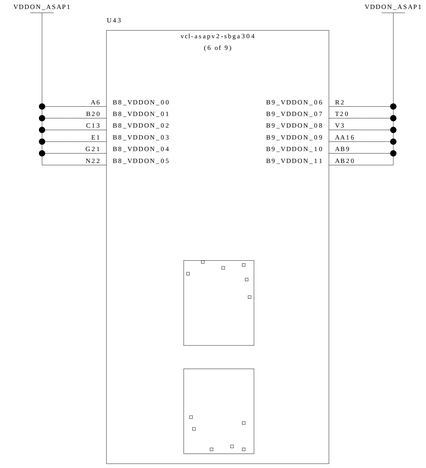
VLSI Computation LAB

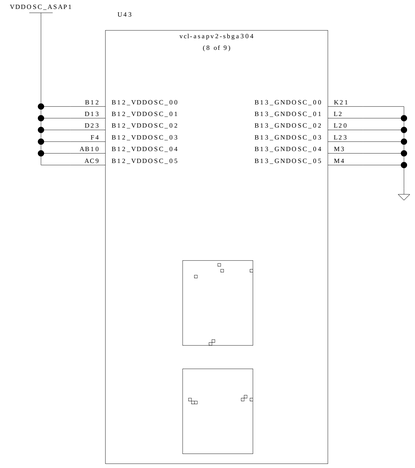
Title:	AGILENT 16902A LOGIC ANALYZER E5390A SOFT-TOUCH CONNECTOR			
File:	MEAS_MAIN_BOARD			
Created by:	JEREMY W. WEBB		Date:	6-20-2008_16:40
Modified by:			Date:	
PCB NO:	342	Size: C	Sheet 37 of 43	REV: 001

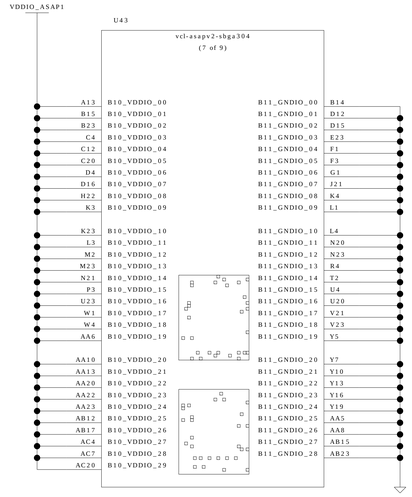
AsAPv2 #1 Power Supply Inputs

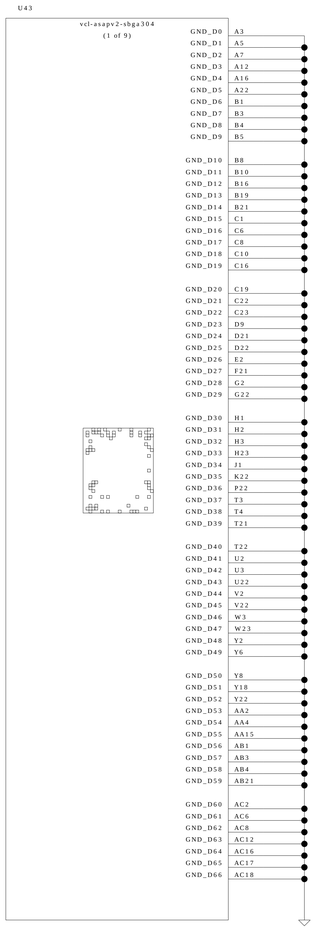








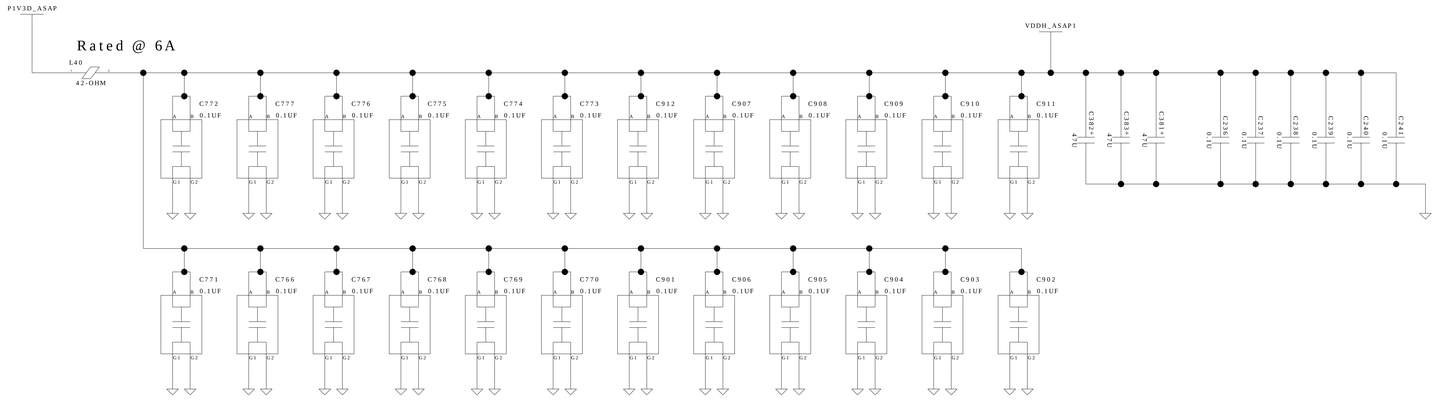


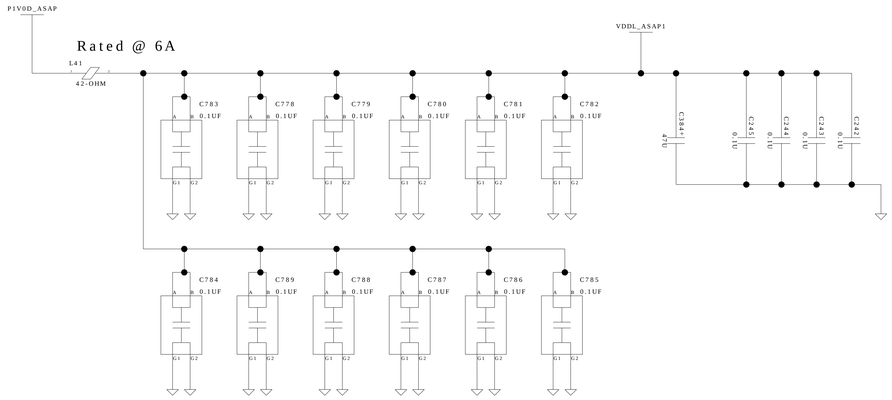


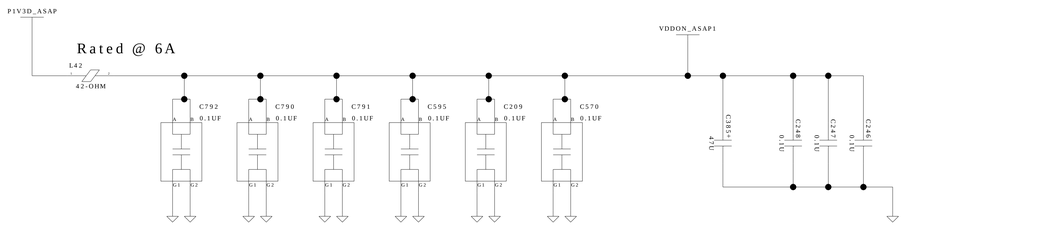
VLSI Computation LAB

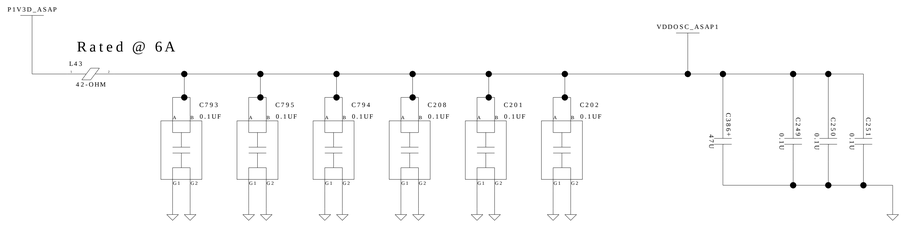
Title:	ASAPV2 #1 POWER SUPPLY INPUTS		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 38 of 43	REV: 001

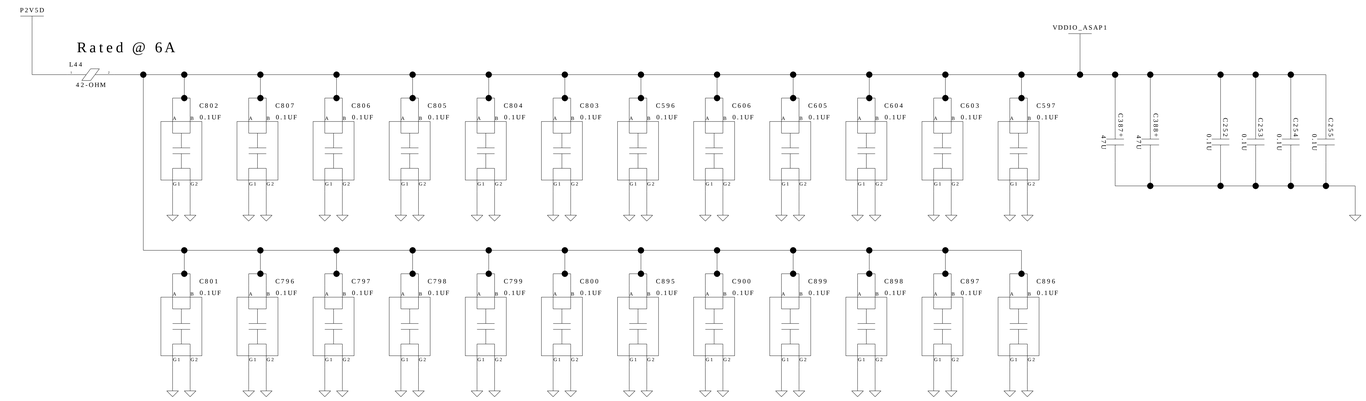
AsAPv2 #1 Power Supply Decoupling





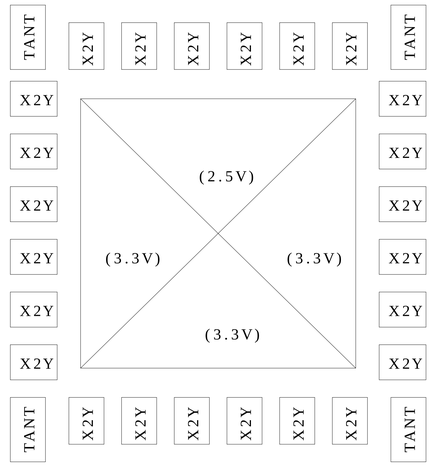






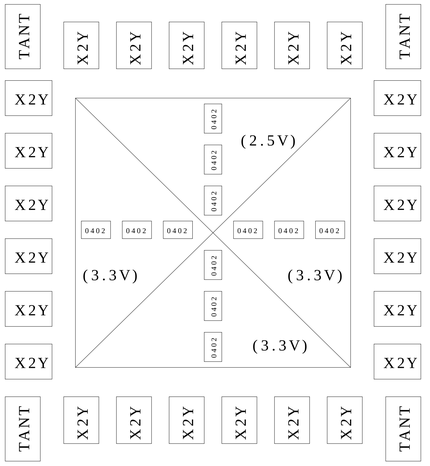
Capacitor Placement

(top side)



Capacitor Placement

(bottom side)



X2Y Capacitor Via Placement

Tantalum/O402 Via Placement

VLSI Computation LAB

Title:	ASAPV2 #1 POWER SUPPLY DECOUPLING		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 39 of 43	REV: 001

AsAPv2 #2 Data In/Out, Config, Analog, Test

** INPUTS **

AsAP 2 Data Output

24-C2,24-E5,40-D4,40-E1 — FPGA_ASAP2_REQ_OUT

AsAP 2 Data Input

24-D2,24-E5,40-D3,40-E1 — FPGA_ASAP2_DATA_IN[15:0]
41-C2,41-C4,41-E1,41-E2
24-D2,24-E5,40-D3,40-E1 — FPGA_ASAP2_CLK_IN
24-D2,24-E5,40-D3,40-E1 — FPGA_ASAP2_VLD_IN
41-C2,41-D1,41-D2

AsAP 2 Config Input

15-B5,15-C3,40-D1,40-E1 — FPGA_ASAP2_RESET_COLD
15-B3,15-B5,40-C1,40-E1 — FPGA_ASAP2_CFG_CLK
15-A5,15-B3,40-C1,40-E1 — FPGA_ASAP2_CFG_VALID
15-A5,15-C3,40-C1,40-E1 — FPGA_ASAP2_SPI_CLK
15-A5,15-C3,40-D2,40-E1 — FPGA_ASAP2_SPI_CSN
15-A5,15-C3,40-C2,40-E1 — FPGA_ASAP2_SPI_LOAD
15-A5,15-B3,40-C2,40-E1 — FPGA_ASAP2_MOSI
14-D4,14-E5,40-B5,40-E1 — FPGA_ASAP2_RST_CNTCLK

** OUTPUTS **

AsAP 2 Data Output

FPGA_ASAP2_DATA_OUT[15:0] — 24-C2,24-D2,24-E1,40-D4 40-E5
FPGA_ASAP2_CLK_OUT — 24-C2,24-E1,40-D4,40-E5
FPGA_ASAP2_VLD_OUT — 24-C2,24-E1,40-C4,40-E5

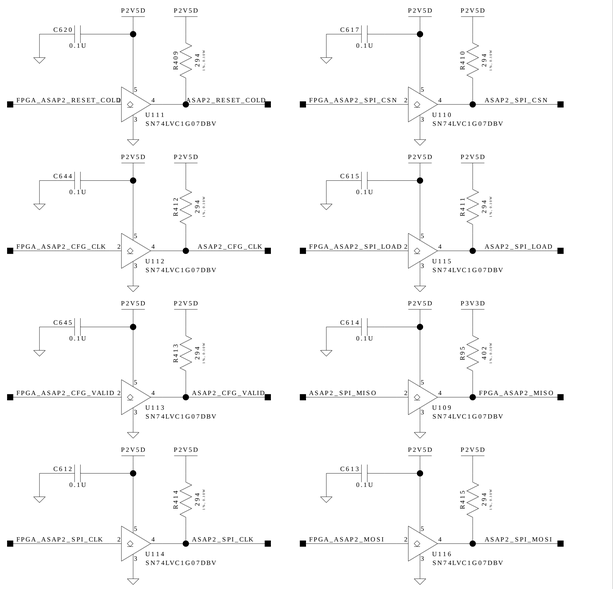
AsAP 2 Data Input

FPGA_ASAP2_REQ_IN — 24-D2,24-E1,40-D3,40-E5

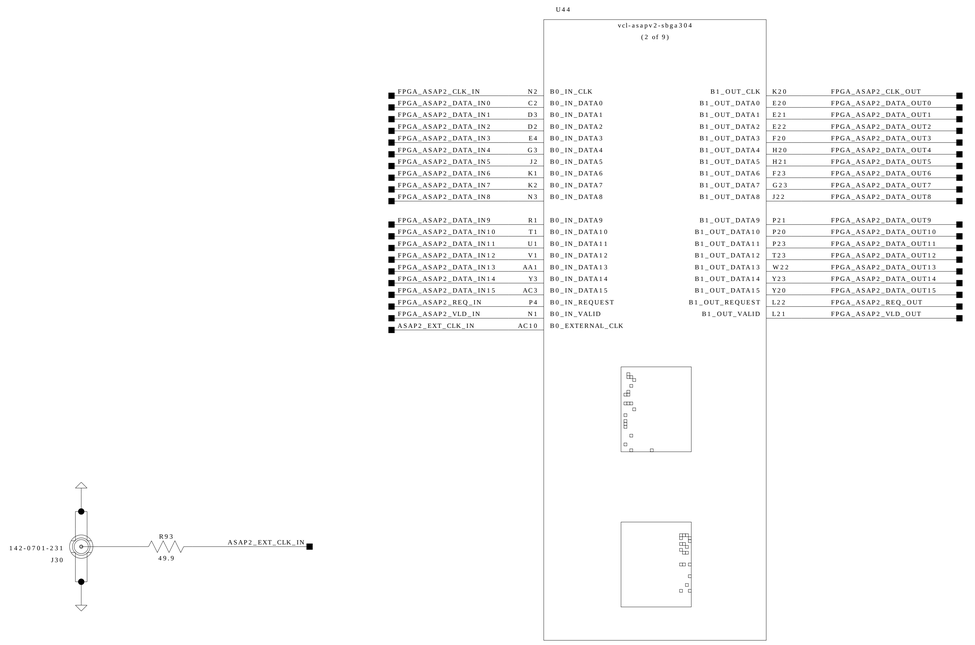
AsAP 2 Config Output

FPGA_ASAP2_MISO — 15-C1,15-C3,40-C2,40-E5

A AsAP Config Level Translate



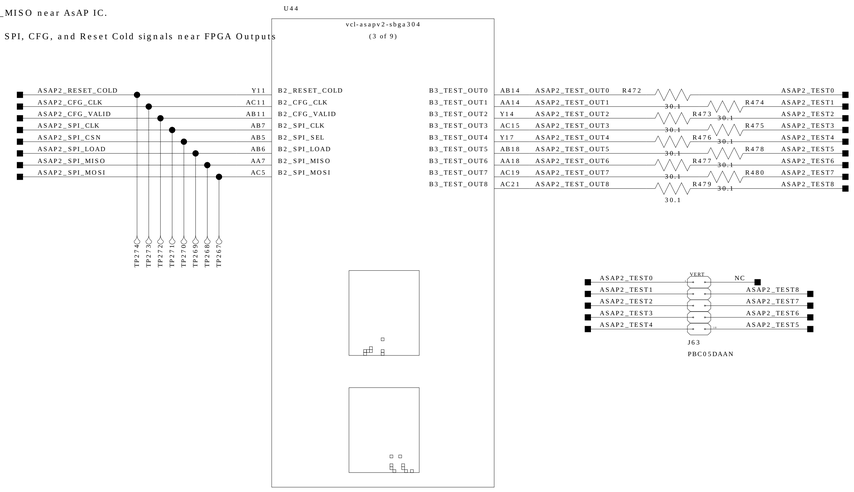
B AsAP Main Data Input and Output



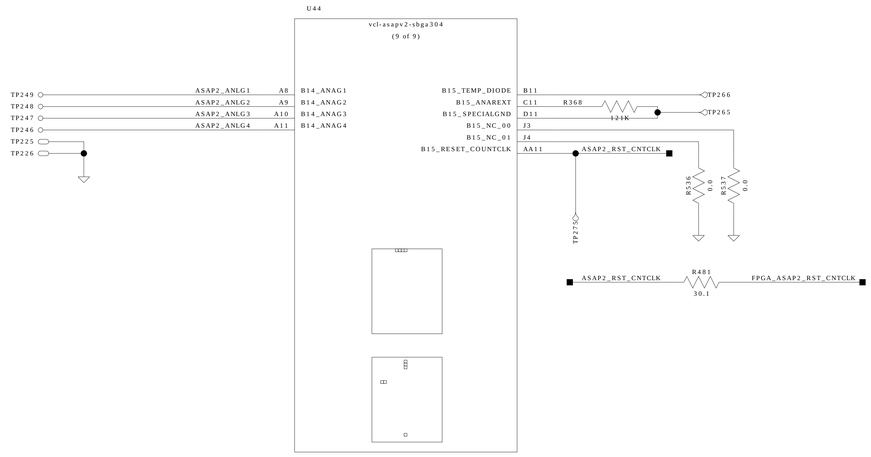
C AsAP Configuration and Test Port

Place 30.1 Ohm Series Resistor on AsAP SPI_MISO near AsAP IC.

Place 30.1 Ohm Series Resistors on all other SPI, CFG, and Reset Cold signals near FPGA Outputs



D AsAP Analog and Miscellaneous I/O



VLSI Computation LAB

Title:	ASAPV2 #2 DATA IN/OUT, CONFIG, ANALOG, TEST		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO:	342	Size: E	Sheet 40 of 43 REV: 001

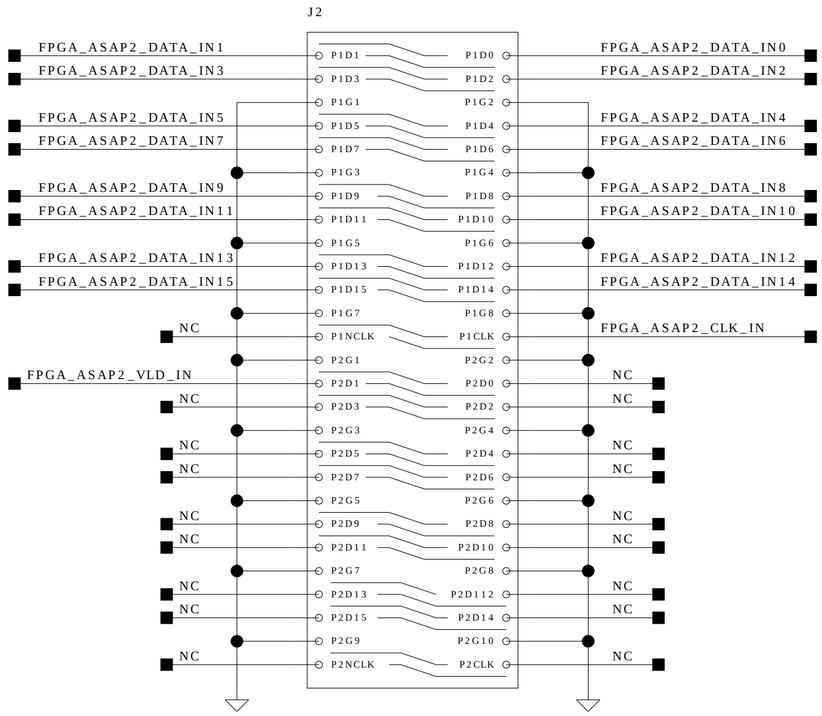
AGILENT 16902A Logic Analyzer E5390A SOFT-TOUCH CONNECTOR

** INPUTS **

AsAP 2 Data Input to Logic Analyzer

A

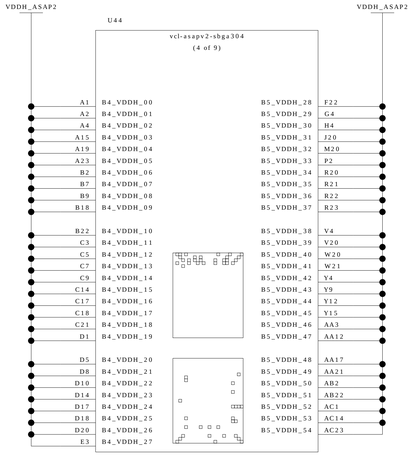
SOFT-TOUCH SINGLE-ENDED PROBE (E5390A)

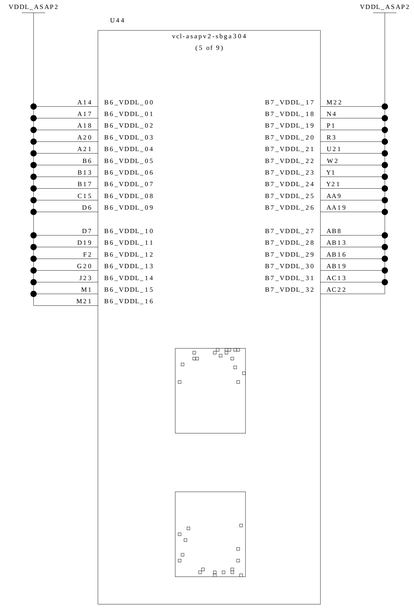


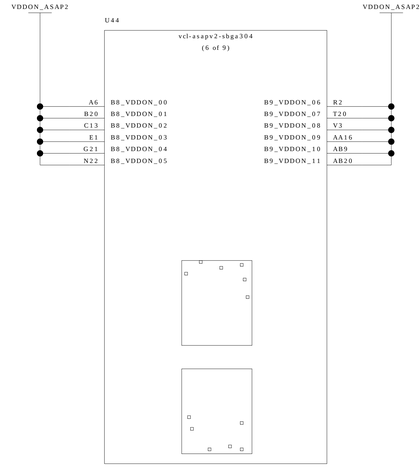
VLSI Computation LAB

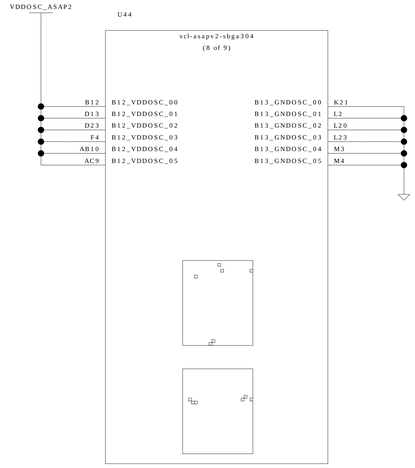
Title:	AGILENT 16902A LOGIC ANALYZER E5390A SOFT-TOUCH CONNECTOR		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: C	Sheet 41 of 43	REV: 001

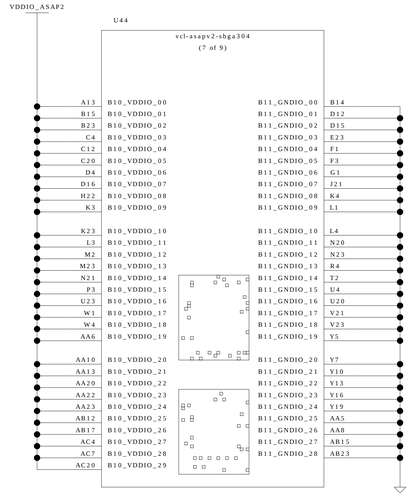
AsAPv2 #2 Power Supply Inputs

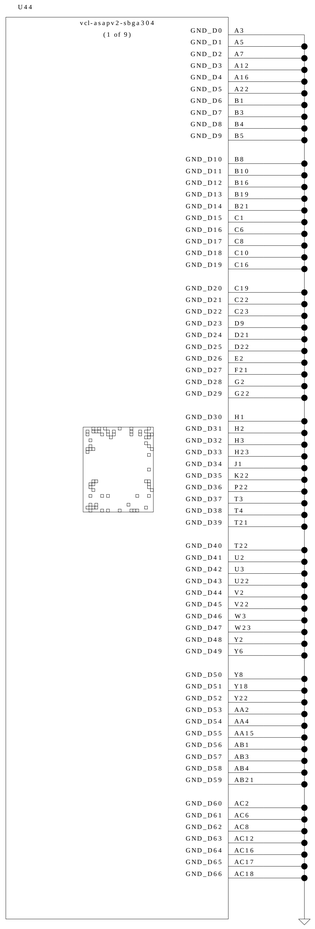








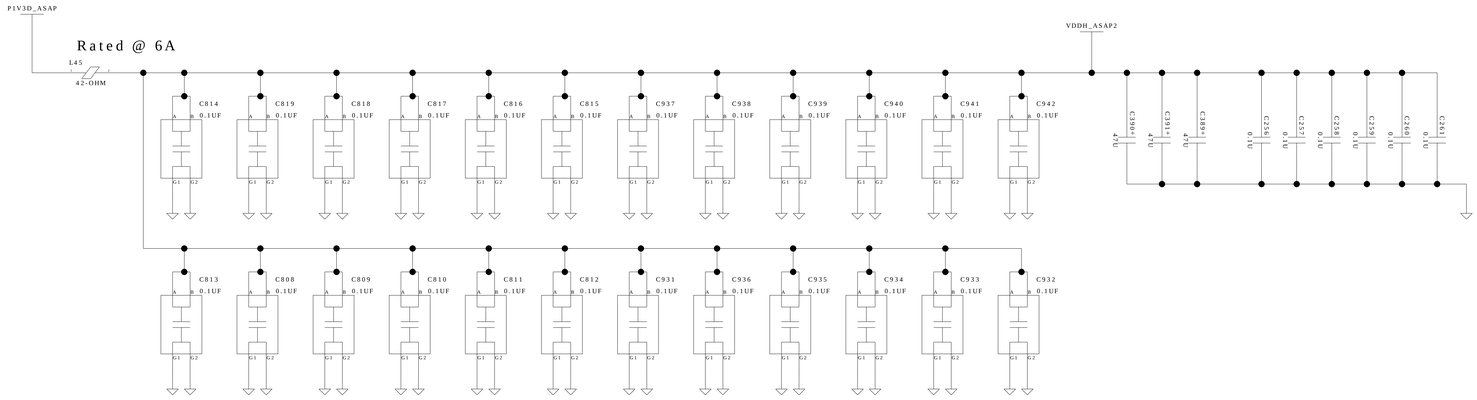


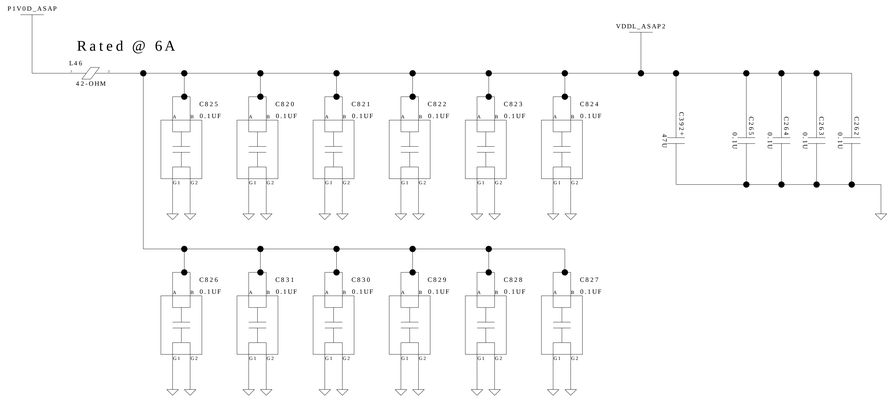


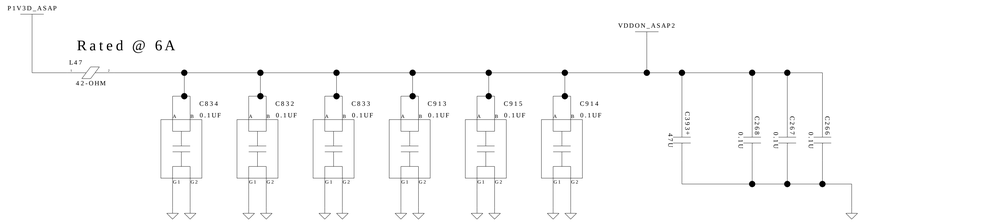
VLSI Computation LAB

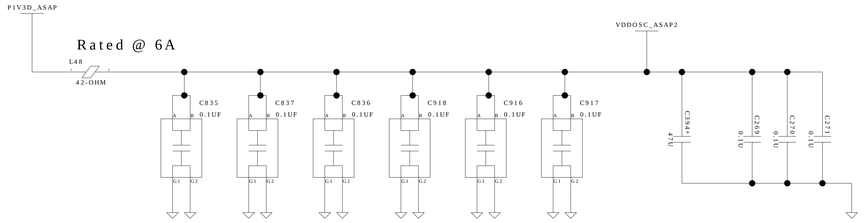
Title:	ASAPV2 #2 POWER SUPPLY INPUTS		
File:	MEAS_MAIN_BOARD		
Created by: JEREMY W. WEBB		Date: 6-20-2008_16:40	
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 42 of 43	REV: 001

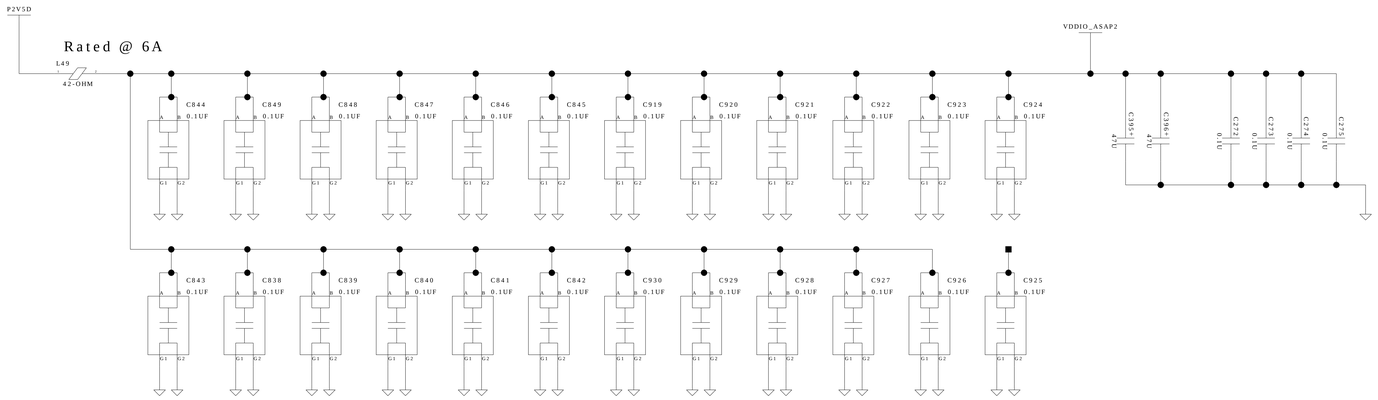
AsAPv2 #2 Power Supply Decoupling



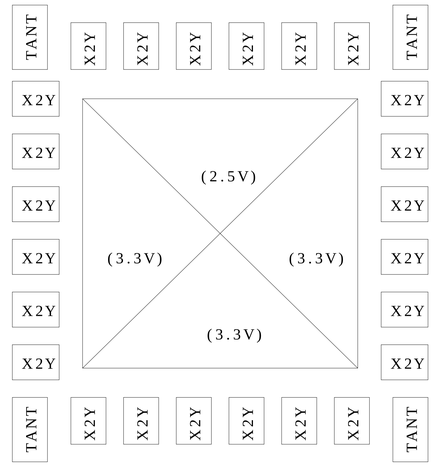




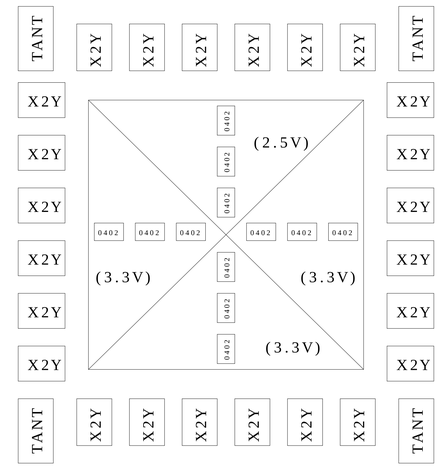




Capacitor Placement (top side)



Capacitor Placement (bottom side)



X2Y Capacitor Via Placement

Tantalum/O402 Via Placement

VLSI Computation LAB

Title:	ASAPV2 #2 POWER SUPPLY DECOUPLING		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	6-20-2008_16:40
Modified by:		Date:	
PCB NO: 342	Size: E	Sheet 43 of 43	REV: 001